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Challenges and Prospects of Nanoscale MOSFET Scaling: A Review

Ahmed S. Al-Jawadi[a], Mohammad Tariq Yaseen[b,c], Qais Thanon Najim[d]
[a] *Department of Electrical Engineering, Collage of Engineering University of Mosul, Mosul, Iraq*
Email: ahmed.salim@uomosul.edu.iq; *ORCID:* https://orcid.org/0000-0003-1306-7485
[b] *Department of Electrical Engineering, Collage of Engineering University of Mosul, Mosul, Iraq*
Email: mtyaseen@uomosul.edu.iq; *ORCID:* https://orcid.org/0000-0001-7173-8684
[c] *Department of Communications and Intelligent Digital Systems Engineering, University of Mosul, Mosul, Iraq*
Email: mtyaseen@uomosul.edu.iq ; *ORCID:* https://orcid.org/0000-0001-7173-8684
[d] *Department of Electronic Engineering, Collage of Electronics Ninevah university, Mosul, Iraq*
Email: qais.najim@uoninevah.edu.iq; *ORCID:* https://orcid.org/0000-0002-6524-946X

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ABSTRACT

The nonstop scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is considered a driving force in semiconductor technology, allowing higher integration densities, enhanced performance, and reduced power consumption. However, fundamental challenges arise as device dimensions shrink to the nanoscale, such as short-channel effects, threshold voltage variation, leakage currents, and gate oxide tunneling. This study critically surveys these scaling limitations and shows potential solutions, such as high-k gate dielectrics, metal gate integration, and novel device architectures. Other transistor designs, including FinFETs, Gate-All-Around (GAA) transistors, and emerging beyond-CMOS devices, are assessed for their potential to extend Moore's Law. This study also addresses advancements in materials, including two-dimensional (2D) semiconductors and carbon-based nanostructures, that offer promising substitutes to conventional silicon technology. Regardless of these innovations, significant obstacles remain in achieving fabrication, reliability, and cost-effectiveness at sub-5nm nodes. This review paper provides insights into current progress and future guide for nanoscale MOSFET development, comprehensively assessing the challenges and opportunities in next-generation transistor technology. The findings aim to guide researchers and industry professionals toward sustainable semiconductor scaling approaches.

1. Introduction

The advancements in MOSFET technology have significantly driven the semiconductor industry's growth for many years. The typical reduction in the size of devices maintains this expansion. The processing capability of MOSFET technology has significantly improved due to downscaling. Device size and supply voltage downscaling have considerably enhanced processing speed and density[1]. Therefore, since the 1960s, gate length

* Corresponding author: Mohammad Tariq Yaseen; mtyaseen@uomosul.edu.iq ; +964-7736977178

has decreased from hundreds of micrometres to a few nanometers. In the 1970s, it became apparent that devices featuring gate lengths of 1 μm were prone to a problematic phenomenon known as the short channel effect. The enhancement of speed and drive current, achieved through scaling down the supply voltage, necessitated reducing the threshold voltage. However, this increased subthreshold leakage, elevating the leakage power [2].

Additionally, reducing the size of the silicon dioxide (SiO2) is necessary to enhance the control of the electrode over the channel and improve the drive current. However, this downsizing is limited to a minimum level of 1.2 nm due to physical constraints and concerns about reliability [3]. Therefore, the ongoing trends in scaling are limited by issues, including the increasing problem of leakage, limited current capability, degradation carrier mobility, cost, and challenges in manufacturing [3]. In order to sustain the historical improvements and address the challenges posed by scaling future technology and minimizing the impact of small geometric effects, researchers have explored and implemented many methodologies and novel device topologies.

This review provides a thorough evaluation of current and future MOSFET technologies. It also discusses the challenges and possibilities in designing MOSFETs with gate lengths below 10 nanometers using a hierarchical framework for MOSFET scaling. The review identifies the most promising logic devices and technologies with gate lengths below 5 nanometers. It highlights the necessary research efforts to concentrate and optimize the research activities in this field.

The paper is organized into five main sections. Section 2 examines recent developments in MOSFET scaling. Section 3 addresses the challenges associated with technological scalability. Section 4 discusses potential solutions to these challenges, including using high-K materials and nanotechnology devices in current and emerging fields. Finally, Section 5 presents the paper's conclusion.

2. MOSFETs Scaling

Enhancing the system's reliability, boosting the current drive, computing power, and the density of integration while reducing costs is crucial through scaling. The strategy of device scaling has been demonstrated to be the most efficient up to this point [4]. Reducing the size of an integrated circuit (IC) results in a greater number of circuits per unit area, increased speed of operation, and reduced power loss[5]. The primary concept that governs initial sizing is to minimize the overall dimensions of transistors, which produces a more compact transistor, aiming to achieve the same or enhanced performance compared to their larger devices [6]. Fig. 1 illustrates the goal of reducing the size of MOS transistors. The configuration shown on the right is scaled down compared to the one on the left, with all dimensions decreased by a factor of α [6].

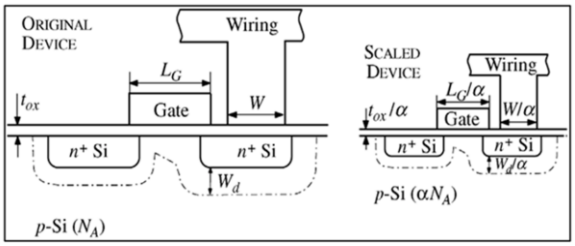


Figure 1. The fundamental concepts behind MOSFET and IC scaling [6].

At first, the length of the MOSFET's gate was measured in micrometers. Nevertheless, the length of the channel has been decreased to the nano-scale [7]. Using scaling MOSFETs in 1974 resulted in advancements in device density, switching speed, and energy efficiency [8]. In 2019, Samsung Electronics and TSMC produced the smallest MOSFETs, 5 nm FinFET semiconductor nodes [9]. Scaling of MOSFETs can improve both processing speed and RF performance [10]. Fig. 2A illustrates the advancement of MOSFET gate scaling technology. Reference [10] demonstrates that as the active power per transition reduces, both the device density and power consumption increase twofold, as shown in Fig. 2B [11]. Consequently, the semiconductor industry has embraced Moore's law and the scaling theory. Fig. 3 illustrates the yearly reduction in dimensions according to the ITRS roadmap [12].

The main reason for shrinking transistors is to increase the density of components on a single integrated circuit, which enables the creation of chips that maintain the same functionalities in a smaller area or offer improved functionalities within the same area. The cost of each integrated circuit mainly depends on the number of chips produced per semiconductor wafer. Therefore, smaller ICs result in a higher number of chips per wafer, reducing the cost of each chip.

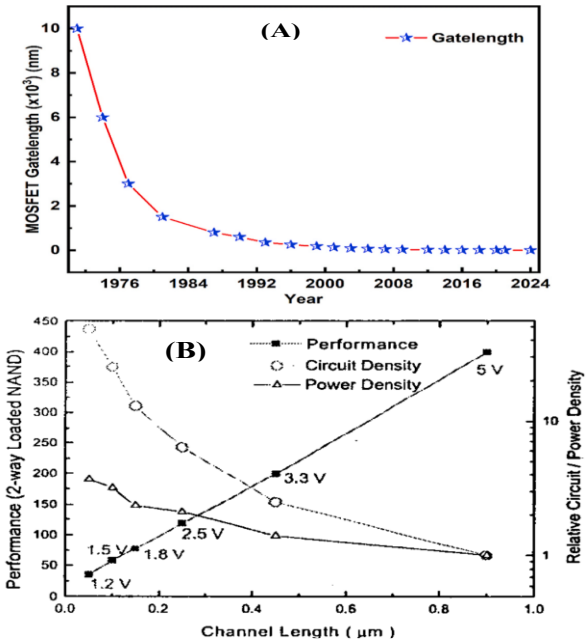


Figure 2. (**A**) Decrease in gate length over the years in VLSI technology [10] (**B**) Power and circuit density trends in CMOS technology [11].

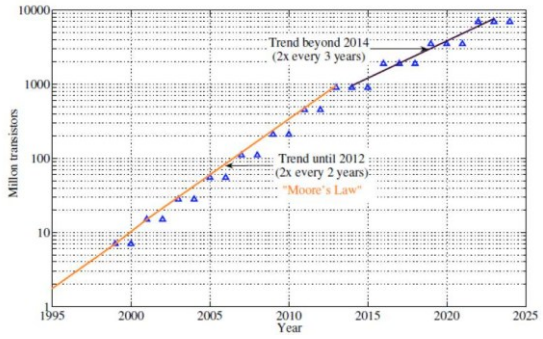


Figure 3. Semiconductor technology road map [12].

3. Significant Challenges in Reducing the Size of MOSFET Devices

Although the production of smaller transistors has advantages such as increased space efficiency, faster speed, and greater performance, it also presents notable problems [9]. These issues arise as the size of the MOSFET is shrunk to the nanoscale, leading to decreasing performance. Hence, it is crucial to tackle these concerns to guarantee the continued viability of MOSFET technology [8].

3.1 Limits for Quantum Tunnelling

Typically, in the field of the design of chips, it is common practice to maintain a sufficient distance between transistors to prevent any interference or disruption between their operations [8]. An intermediate substance is inserted between transistors to create a separation and serve as a barrier. However, as MOSFETs are scaled down, the barrier between transistors also shrinks. Consequently, the probability increases for one transistor to influence the performance of another since carriers can migrate between them [8, 13].

3.2 Effects on Short Channels

A MOSFET is described as being in a short-scaled condition when the length of its channel is equivalent to the widths of the depletion layers in the source and drain regions beneath the gate and if a potential differential between the drain and source is zero. When the size of a device decreases dramatically, short channel effects become dominant and affect the device's performance. A significant obstacle in the nano-scale domain is reducing short-channel effects while preserving optimal device performance[10].

3.2.1. Drain Induced Barrier Lowering

Drain-induced barrier lowering, DIBL, occurs when the voltage at the drain of a MOSFET reduces the potential barrier between the source and channel regions. In devices with long channels and perfect features, the gate voltage is the primary means of controlling the potential barrier. Nevertheless, as the length of the transistor channel decreases with each technological progress, the impact of the drain voltage on this barrier has grown more significant. It is essential to analyze the electric fields within the device. As the voltage delivered to the drain increases, an electric field that extends throughout the channel is created. This field greatly reduces the potential barrier electrons must surpass from the source to the drain. Consequently, even when the transistor is intended to be in an off-state, the reduced barrier allows more electrons to flow, leading to higher off-state currents and less channel control by the gate voltage [14]. DIBL significantly impacts the threshold voltage of the transistor, making it one of the most prominent impacts. The magnitude of DIBL is closely connected to the reduction in transistor dimensions. The impact becomes more evident as the channel length decreases[14]. Equation 1 is used to calculate the DIBL, where ΔV_{th} is the change in threshold voltage concerning the drain source voltage (V_{ds}), and the V_{th1}, V_{th2} are the threshold voltages obtained at low

drain voltage (V_{dS1}) and saturation drain voltage (V_{ds2}) respectively[15].

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{ds}} = \frac{(V_{th2} - V_{th1})}{(V_{ds2} - V_{ds1})} \quad (1)$$

3.2.2. Surface Scattering

Surface scattering or Hot Electron Effects is a fundamental concept in semiconductor physics that has become more significant as electronic devices shrink to nano-scale dimensions. The phenomenon is the interaction between charge carriers and a material's physical boundaries or interfaces due to electrons gain substantial kinetic energy when subjected to high electric fields. This interaction is critical in determining contemporary semiconductor devices' electrical properties and operational efficiency. When electronic devices get smaller, the scattering of carriers at the surface of the device becomes more significant compared to scattering inside the device's body. This change has great ramifications for the movement and ability to conduct electricity of substances, especially in small structures, such as thin films, nanowires, and quantum dots. Surface scattering is affected by many parameters, such as surface roughness, defects or impurities, and the energy and momentum of the charge carriers[16].

3.2.3. Velocity Saturation

There is a substantial influence that velocity saturation has on the performance of modern electronic devices, particularly in high-speed and miniaturized transistors. There is a correlation between the size of semiconductor devices and their ability to operate at higher electric fields, and the relevance of this phenomenon rises as the size of devices reduces. In the natural environment, the velocity of electrically charged particles in a semiconductor would exhibit a linear rise in proportion to the strength of the electric field. According to [17], this linear association only applies until a threshold is exceeded. Once the threshold is exceeded, the velocity of the carrier deviates from linear patterns and achieves its maximum value, which is referred to as the saturation velocity.

Velocity saturation arises from the interactions between charge carriers and the semiconductor crystal lattice and may be attributed to a physical process. When exposed to strong electric fields, carriers absorb energy from the field more quickly than they can transfer it to the lattice. The lack of balance in this state leads to a shift in energy allocation across carriers, resulting in a preference for higher energy levels. As a result, the probability of encountering further scattering processes that restrict the velocity of carriers is increased. Velocity saturation substantially affects semiconductor device design and operation, especially in short-channel MOSFETs. The researchers in [18] reported that this phenomenon restricts the upper limit of current, transconductance, output resistance, and frequency responsiveness. So, Comprehending and considering velocity saturation is crucial in contemporary semiconductor device modeling and simulation. The velocity saturation effect governing the drain current in the saturation region is expressed by Equation 2. Where μn is the carrier mobility, Cox is the oxide capacitance, W and L are the Width and length of the MOSFET channel, and Ec is the critical electric field for velocity saturation[19].

$$I_d = \left[\frac{1}{2}\,\mu_n\,C_{ox}\,\frac{W}{L}\,(V_{gs} - V_{th})^2\right]\left(\frac{1}{1+\frac{V_{gs}-V_{th}}{E_C L}}\right) \quad (2)$$

3.2.4. Oxide Tunneling Current

Oxide tunneling current is a quantum mechanical effect in modern semiconductor devices, especially in thin-gate-oxide MOSFETs. It significantly influences leakage current (I_{off}) during the OFF state, posing power efficiency and performance challenges[20, 21]. This phenomenon results from shrinking device dimensions, altering electric fields, and electrostatic control. As gate oxide thickness (t_{ox}) decreases, electrons can tunnel through the oxide, increasing gate leakage. Additionally, short-channel devices experience diminished gate control, leading to greater subthreshold leakage. The drain voltage lowers the source-channel barrier, allowing more carriers to flow when the device is OFF. The leakage current can be mathematically represented in Equation 3[22].

$$I_{off} = 100\frac{W}{L}\,10^{\frac{-V_{th}}{SS}} \quad (3)$$

The subthreshold swing, represented as SS, measures the efficiency of a transistor's transition from ON to OFF state. An ideal value is approximately 60 mV per decade at room temperature. However, this value typically deteriorates in miniaturized devices due to insufficient electrostatic control. Equation 4 represents the mathematical relationship of SS, where Cd is the depletion capacitance[15].

$$ss = 60(1 + {}^{C_d}/_{C_{ox}}) \quad (4)$$

3.3 Practical Difficulties in Implementing Nanoscale Devices

The development of nanoscale MOSFETs presents other practical challenges. Variability in the manufacturing process can lead to inconsistencies in lithography and doping, which in turn causes fluctuations in threshold voltage and overall device performance. Additionally, defects and errors in lithography contribute to yield challenges, resulting in fewer functional devices. The cost of production is also impacted by the need for advanced tools, such as EUV lithography and high k materials, making the manufacturing process more expensive. Addressing these challenges demands innovative fabrication techniques and rigorous process controls to ensure reliability and cost-efficiency in the production of nanoscale devices [23].

4. Solution of Short Channel Effects (SCEs) Challenges

Short channel effects, SCEs, have emerged as serious issues due to the constant growth of semiconductor devices, especially MOSFETs. The impact of these phenomena becomes increasingly significant when transistors decrease in size to nano-scale dimensions, which has the potential to undermine device performance, escalate power consumption, and diminish dependability. In order to tackle these problems and sustain the rate of progress in integrated circuit technology, the semiconductor industry has devised a variety of inventive remedies. These methods focus on different areas of device design and production to reduce the effects of SCEs while allowing for further downsizing. Understanding and applying these solutions helps the semiconductor industry overcome scaling restrictions and increase the performance and efficiency of electronic devices in numerous applications. As explained in the following:

4.1 Dielectrics with High k

High dielectric constant oxides are insulating materials composed of essential binary and ternary compounds of materials. They are characterized by a high dielectric constant, typically greater than 9. These materials notably incorporate transition metals from groups 3 to 5, aluminum, and lanthanides[24]. In recent years, significant advancements have been witnessed in the identification and understanding of physical characteristics. The materials include metal oxides from group IIIA, for example, material oxides, aluminum oxide (Al2O3) and silicates from group IVB, such as titanium oxide (TiO2), lanthanum oxide (La2O3), zirconium oxide (ZrO2), strontium titanate (SrTiO3), Hafnium oxide (HfO2), tantalum oxide (Ta2O5) and yttrium oxide (Y2O3) [24]. The main reason for substituting SiO2 with other gate dielectrics is to minimize gate leakage and allows for decreases in the gate dielectric thickness while maintaining a consistent electric field across the channel. Research indicates that these high k dielectrics significantly reduce direct-tunneling gate currents compared to SiO2, leading to lower power consumption while maintaining equivalent thickness. There is a growing interest in alternate gate dielectrics with higher permittivity to improve low-power technology further[25]. Choosing an oxide with a high dielectric constant requires several specific criteria.

4.1.1. Offset and Gap Band

The K value is the first key requirement that must be suitable value to provide economic viability for many scaling nodes. The oxide dielectric constant should surpass 9, generally 25–35 [26]. The High k oxide must act with a band gap above 5eV. Additionally, each band should have a potential barrier of at least 1eV, this requirement is crucial for minimizing the carrier injection into the oxide bands through Schottky emission, which otherwise results in unacceptably high leakage currents. Table 1 provides a detailed overview of the dielectric materials, their specific k values, band gap (Eg), and the conduction and valence band offset values. For example, Silica has a band gap of 9 eV, resulting in significant electron and hole barriers. The conduction band offset of Si is 3.9eV, whereas its valence band offset is 4.7eV. Nevertheless, the conduction band offset is much reduced for oxides, which have a more limited difference in energy levels between the valence and conduction bands, such as SrTiO3, Ta2O5, and TiO2. For the energy barriers to be more than 1eV, the alignment of these oxide bands about those of silicon must be almost symmetrical. A balance is also to be struck between the value of k and the offset of the band. High-k dielectrics usually show a reverse correlation between their k value and band

gap. The energy of the band gap in metal oxides often drops as the atomic number goes up, as shown in Fig. 4 [27].

Table 1. Physical features of dielectrics [27].

Dielectrics	Energy gap(eV)	Dielectric constant	Valance bandoffset (eV)	Conduction band offset (eV)
SiO2	9	3.9	4.7	3.2
HfO2	5.8	25	3.3	1.4
SrTiO3	3.2	2000	2.1	0
Al2O3	8.8	9	4.8	2.8
TiO2	3.5	80	2.4	0
Ta2O5	4.4	22	2.95	0.35
Si3N4	5.3	7	1.8	20.4
La2O3	6	30	2.6	2.3
ZrO2	5.8	25	3.2	1.5

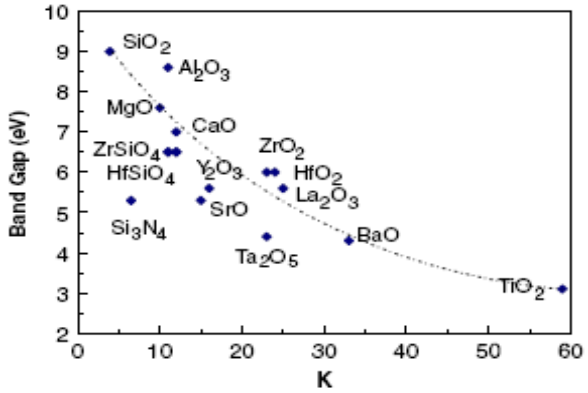


Figure 4. Various dielectric constants against band gaps [25].

4.1.2. Quality of the Channel Interface

The connection between the channel and dielectrics is essential for improving applications' MOS functioning. The bonding restrictions are indicated to impact the quality of the Si-dielectric contact[28]. If a material has more or fewer bonds per atom than Si, the number of defects at the boundary will similarly rise. Moreover, the deposition of materials on a Si substrate under equilibrium conditions will likely result in an unwanted and unregulated Interface layer[28]. Therefore, an interfacial reaction barrier is essential for enhancing the quality of the channel interface. To effectively manage and improve the quality of the channel interface, it is essential to know how the gate dielectric interacts with silicon, the movement of oxygen, the composition of oxygen, the formation of the film's crystals, and the separation of its components during subsequent processing [28].

4.2 Metallic Technology for Gates

In order to lessen the fluctuations in the intrinsic parameters, high-k/metal gate technology was used. Because the work function depends on the orientation of the metal grains, using metal as a gate material introduces a third source of random variation. According to the findings presented in [29], The fluctuations in intrinsic parameters, variations in metal gate work function, effects of process variation, and random dopant fluctuations significantly influence the DC/AC, as well as the timing, power, and high-frequency performance of 16nm-gate bulk MOSFETs. This extensive investigation evaluates the variations in digital circuit performance and reliability.

4.3 Lateral Channel Engineering

Halo profiles efficiently augment the average doping concentration in shorter field-effect transistors (FETs) channels compared to longer channel FETs. Consequently, this action neutralizes the reduction in Vth resulting from short-channel effects. Halos like these enable 25nm bulk CMOS. Advantages of alternate device topologies include a considerably higher ideality factor, and thinner silicon channels than bulk devices, unless they are in extremely low temperatures [30]. This method provides additional flexibility in attempts to mitigate the negative consequences of SCE. The source and drain connections channels have been reshaped utilizing lateral channel engineering techniques, including tilted channel installation, Halo pocket, and tilted insertion punch-through blocker, which involve locally increasing the doping concentrations[30].

4.4 Gates with Extreme Doping

The severity of poly depletion effects will intensify when MOSFETs are further downscaled, primarily attributed to the importance of corner and edge impacts. To successfully address these issues, it is advisable to choose gates that have a high doping level and a low dopant differential in the poly gate. The length of the depletion region increases for shorter gate lengths, resulting in a larger potential fall. This method uses device modeling to explain the influence of irregular dopant distributions and gate shape on the impact of poly depletion. The existence of uneven and sharp dopant profiles in the poly-gate manifests inherent electric field

impacts and depressions in the gate area. The presence of evenly spread and curved dopant distributions within the poly-gate leads to significant drops in potential at the edges for small gate lengths, primarily because of fringing fields [31].

4.5 Scalability-Related Technologies to Resolve the Challenges

Materials and structural design improvements have solved scaling issues [32].However, it is expected that meeting the demands of MOSFET technology with traditional planar MOSFET configurations will become increasingly difficult after 2007, despite introducing high dielectric constants, metal gate electrodes, and other progressive techniques [33].Active research in both academic and commercial settings has been directed toward exploring new materials and designs to overcome challenges associated with scaling [33]. Efforts to extend the viability of Moore's Law have taken several directions, such as enhancing electrostatic control over the transistor channel by reducing the equivalent oxide thickness via a high-k dielectric with metal gate stack and adopting multiage structures to improve drive currents while keeping the over operation voltage (VDD-Vth) constant. Moreover, there have been advancements in increasing carrier mobility through the use of high mobility channel materials and the application of the strain engineering .Innovations have led to the development of various transistor models, including Silicon on insulator Planar double gate MOSFET, Tunnel field effect transistor, Fin field effect transistor, Gate all around FET, Tunnel field effect transistor, and nanowires or carbon nanotubes [33].

4.5.1. Silicon on Insulator

The benefits of SOI technology are rooted in its buried oxide layer. A cross-sectional view of an SOI device is depicted in Fig. 5; SOI devices boast enhanced switching speeds and lower power consumption by reducing parasitic capacitances, namely the drain/source junction capacitances. [34].
SOI transistors can be classified into two main types: partially depleted PD-SOI and fully depleted FD-SOI. PD-SOI transistors are defined by having a silicon film on the Buried Oxide layer thicker than the depletion region beneath the gate oxide, typically exceeding 100nm. On the other hand, FD SOI transistors feature a significantly thinner silicon body, usually less than 50nm, or are lightly doped, enabling the entire body to be depleted. Fully depleted ultrathin-body SOI devices are highly regarded as one of the most effective solutions for scaling due to their meticulous device design and innovative production techniques. SOI technology allows for higher transistor density and streamlines the manufacturing process [35].
Furthermore, there is a significant drawback associated with SOI technology. The BOX, with a thermal conductivity about 100 times lower than Silicon, is an obstacle that hinders the flow of heat from the SOI transistors to the substrate. Consequently, the SOI transistors are highly vulnerable to the thermal heating generated in the channel, manifesting "Self-Heating Effects" [35].

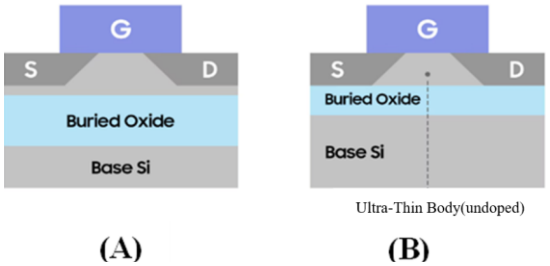


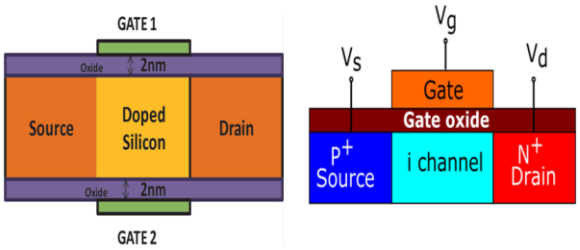
Figure 5. Cross section of (A) PDSOI (B) FDSOI MOSFET [36].

4.5.2. Double-Gate MOSFET

A double-gate MOSFET employing planar fabrication methods has been developed, featuring a drain-source channel sandwiched precisely between two sets of gate oxides, as depicted in Fig. 6A [37]. This structure enables enhanced control over the channel potential, resulting in diminished short-channel effects such as DIBL and velocity saturation, especially in nanoscale technologies. DG MOSFETs offer increased drain current capability and a better subthreshold slope, making them well-suited for high-performance applications. Recent research has produced analytical solutions and compact models for DG MOSFETs. In 2024[38], researchers incorporated high k dielectrics, examined strain engineering, and adopted multi-gate architectures to mitigate short-channel effects. Additionally, Researchers in 2023[39]have explored quantum confinement mechanisms and integrated 2D materials to enhance carrier mobility while lowering power consumption. These features set DG MOSFETs as essential components in the future of integrated circuit designs.

4.5.3. Tunnel Field Effect Transistor

Substantial progress has been made in developing Tunnel Field Effect Transistors. TFETs' unique characteristic is their use of the band-to-band tunnelling process, which enables them to reach a low subthreshold swing (SS) [40] ; this is facilitated by doping the drain and the source regions of a TFET with opposite-polarity dopants, as illustrated in Fig. 6B.



(A) **(B)**

Figure 6. Cross-section of (A) DG-MOSFET [41] (B)TFET structure [42].

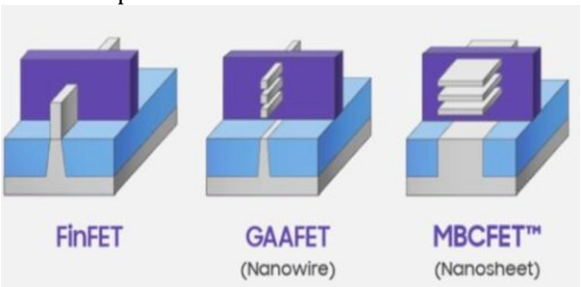
BTBT, also known as band-to-band tunneling, occurs when the application of gate voltage to a junction between the source and channel results in a narrow tunneling width, allowing electrons to flow across via tunneling. Reference [40] states that the Tunnel FET can achieve a sub-kT/q (sub-threshold) swing Because of the influence of BTBT. The TFET has the advantage of having an exceptionally low leakage current I_{off} , along with a high I_{on}/I_{off} ratio . TFET exhibits characteristics that make it a viable alternative to MOSFET in applications that need low power consumption and high frequencies. TFET faces limitations, such as a lower ON current and ambipolarity, which hinder its practical application in circuitry, thereby delaying its extensive commercial deployment[40]. Given the significant advancements in Tunnel Field-Effect Transistor (TFET) technology, various researchers are exploring different TFET configurations, including double-gate, FinFET, and gate-all-around. Nonetheless, implementing these TFET architectures poses notable challenges when moving beyond the 32 nm node due to manufacturing limitations. The challenges primarily stem from integrating p+source and n+drain regions within their structural designs[43].

4.5.4. Fin Field-Effect Transistor (FinFET)

The FinFET is an advancement in transistor technology that addresses the limitations of planar MOSFETs as semiconductor technology advances to process nodes. It was first introduced in the 1989s by Hitachi Central Research Laboratory[44]. FinFETs have become integral to modern semiconductor manufacturing. The distinctive tridimensional design enables the gate to surround three channel sides, leading to electrostatic control, as shown in Fig. 7A. This enhanced regulation addresses short channel effects, a problem encountered in transistors that can lead to increased power consumption and reduced performance [44].

FinFETs are not solely focused on improving channel control. Their design permits a flow of current in a space, resulting in the creation of more robust and effective chips. These chips can function effectively at reduced voltages while maintaining high performance, leading to decreased power consumption, which is important in mobile and high-performance computing.

FinFETs are utilized in several applications, one of which is the Polaris GPU architecture using a 14 nm process. This architecture is specially engineered to enhance the performance of graphics cards [45]. In March 2017, Samsung, in collaboration with Silicon, unveiled the creation of a 14nm FinFET ASIC featuring a 2.5D integrated package [46]. According to [47] in 2024, Yalung and his teams created Novel FinFET architectures incorporating strained silicon germanium channels, demonstrating a 22% performance improvement with sub-5nm nodes. FinFETs have transformed semiconductor technology by allowing faster, more efficient, and more powerful electronic devices despite the limitations of complicated 3D designs and increased production costs.



(A) **(B)** **(C)**

Figure 7. Three-dimensional schematic of (A) FinFET (B) GAA. (C) MBCFET [48].

4.5.5. Gate-All-Around FET (GAAFET)

A Gate-All-Around Field-Effect Transistor shares a similar conceptual framework with FinFETs, with the distinct characteristic that the channel region is entirely encased by gate material. GAAFETs can feature a dual-gate or quad-gate configuration based on the specific design goals. They have

demonstrated success in theory and practical experimentation [49]. Fig. 7B illustrates the structural variances between FinFETs and GAAFETs.

Moreover, GAAFETs have been successfully manufactured on Indium gallium arsenide (InGaAs) nanowires, demonstrating superior electron mobility compared to silicon [50]. GAAFETs, or Gate-All-Around Field-Effect Transistors, can operate at dimensions below 7 nm. Consequently, they might be categorized as the succeeding iteration of transistors, exceeding FinFETs. Fujio Masuoka, known for his groundbreaking contributions to the development of flash memory technology, founded Unisantis Electronics in 2004 following his departure from Toshiba. This partnership with Tohoku University aimed to investigate the technologies used in surrounding gates. Gallium Arsenide Field-Effect Transistors (GAA FETs) offer an advantage in the precise regulation of electrostatics. The unique design of these transistors efficiently minimizes leakage current and effectively addresses short-channel effects, surpassing the performance of FinFETs. This characteristic enables a continuous decrease in the size of transistors while simultaneously maintaining or enhancing performance and power efficiency. In 2006, Korean scientists successfully developed a 3 nm transistor, making it the smallest nanoscale semiconductor known at that time [51]. In 2024, a team of researchers introduced a multi-stacked nanosheet GAA design at a 3nm node. This innovation reduced parasitic capacitance by approximately 30% while preserving outstanding subthreshold slope properties[52].

4.5.6. Multi-Bridge Channel Field-Effect Transistors

In addition to the Previous structures, there has also been a significant advancement in semiconductor technology, such as Multi-Bridge Channel Field-Effect Transistors (MBCFET), as shown in Fig. 7C. The MBCFET is a breakthrough in transistor design, featuring vertically stacked nanosheet channels that enhance electrostatic control and increase drive currents. This three-dimensional (3D) architecture addresses the challenges faced by FinFETs at sub-3 nm technology nodes, leading to better performance and greater power efficiency. MBCFETs are expected to be essential for developing next-generation logic and memory devices, especially in high-performance computing and artificial intelligence applications. Their capability to scale while consuming less power makes them crucial for advancing future semiconductor technologies[53].

4.5.7. Carbon Nanotube Field-Effect Transistors (CNTFETs)

Metallic nanotubes are highly regarded for their potential as interconnects in future technologies due to their exceptional characteristics, including their ability to carry large currents, outstanding mechanical and thermal strength, and superior thermal conductivity [54]. Additionally, semiconducting nanotubes offer distinct benefits when employed as channel materials in high-performance FETs. The compatibility of carbon nanotube field-effect transistors (CNTFETs) with high-k dielectrics, owing to their lack of dangling bonds, is a noteworthy advantage. Furthermore, the similar current-voltage (I-V) behavior observed in both NMOS and PMOS transistors presents a considerable benefit for CMOS circuit design. Several factors further enhance the appeal of CNTFETs to the silicon-based semiconductor industry: they demonstrate significant enhancements in device performance metrics, such as lower power usage and faster operational speed, and they share operational principles and structures with silicon-based CMOS transistors, allowing for the application of existing CMOS design architectures[54].

Although CNT-based electronics have considerable potential, several intricate challenges must be tackled. Existing techniques for synthesizing or growing nanotubes cannot create tubes with consistent diameters and chiralities. If developing more precise growing processes is impossible, the starting material must be purified. Multiple breakthroughs are being documented in the domain of purification. Additionally, constructing the device demands stricter gate control through ultrathin high dielectric constants and extremely sharp doping profiles [55]. Fig. 8 shows the Schematic view of CNTFETs structure.

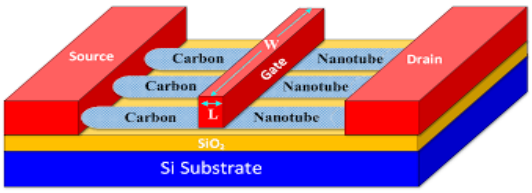


Figure 8. Schematic view of CNTFETs structure [56].

Based on the considerations discussed earlier and a detailed analysis of the factors influencing MOSFET characteristics, we propose a novel

structure distinguished by its simplicity and nanoscale dimensions, as illustrated in Fig. 9 [57]. This design demonstrates promising performance metrics, achieving an ON current of approximately 2.361 mA/μm while significantly reducing the OFF current to 0.1326 nA/μm. Additionally, it effectively mitigates short-channel effects, as evidenced by a Drain-Induced Barrier Lowering (DIBL) value of 18.26 mV/V. The structure also exhibits a high switching speed, with a subthreshold swing of approximately 66 mV/dec and an Ion/Ioff ratio of 22.85 × 10^6, underscoring its suitability for low-power and high-speed applications.

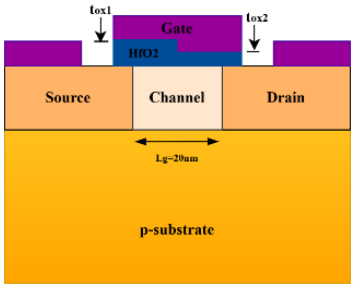


Figure 9. Cross-sectional view of the presented structure.

5. Conclusion

The The continuous scaling of MOSFETs has supported significant advancements in semiconductor technology. Despite its advantages, it has also presented significant obstacles, especially at the nanoscale. Short-channel effects, performance degradation, and the cost and intricacy of manufacturing are critical challenges that need the investigation of innovative materials and device designs. DGMOSFETs provide improved electrostatic regulation and reduced leakage currents. SOI technology also provides enhanced isolation and reduced leakage, but at an increased wafer cost and potential self-heating complications. TFETs have ultra-low power consumption and a steep subthreshold slope; yet, they face challenges with low ON-current and susceptibility to fluctuations. FinFETs effectively reduce short-channel effects and enhance driving currents; nonetheless, they face issues associated with self-heating and manufacturing complexities. GAAFETs offer superior electrostatic control and scalability; however, their production techniques are notably intricate. CNTFETs have exceptional mobility and thermal conductivity, although they encounter challenges stemming from manufacturing discrepancies. The increasing costs associated with the design and manufacturing of modern VLSI chips have led the semiconductor industry to proceed cautiously when adopting new technologies. Consequently, it is necessary to reconsider the traditional MOSFET structure, which is characterized by simplicity, ease of manufacturing, and cost-effectiveness. Moreover, it is necessary to find methods to enhance its performance. A novel MOSFET configuration presented, characterized by an asymmetric oxide gate that includes high-k dielectric material. The proposed gate architecture efficiently modifies the electric field distribution inside the channel, enhancing control over the channel area and positioning it as a feasible substitute for conventional MOSFETs in low-power, high-speed applications, especially at the nanoscale.

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Conflicts of Interest

The authors declare no conflict of interest.

References

[1] K. S. Kim *et al.*, "The future of two-dimensional semiconductors beyond Moore's law," *Nature Nanotechnology,* vol. 19, no. 7, pp. 895-906, 2024.

[2] W. Haensch *et al.*, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development,* vol. 50, no. 4.5, pp. 339-361, 2006.

[3] Y.-B. Kim, "Challenges for nanoscale MOSFETs and emerging nanoelectronics," *transactions on electrical and electronic materials,* vol. 11, no. 3, pp. 93-105, 2010.

[4] V. K. Sharma and M. Pattanaik, "VLSI scaling methods and low power CMOS buffer circuit," *Journal of Semiconductors,* vol. 34, no. 9, p. 095001, 2013.

[5] H. Emami-Nejad, A. Mir, Z. Lorestaniweiss, A. Farmani, and R. Talebzadeh, "First designing of a silicene-based optical MOSFET with outstanding performance," *Scientific Reports,* vol. 13, no. 1, p. 6563, 2023.

[6] Q. Zhang, Y. Zhang, Y. Luo, and H. Yin, "New structure transistors for advanced technology node CMOS ICs," *National Science Review,* vol. 11, no. 3, p. nwae008, 2024.

[7] R. K. Ratnesh, A. Goel, G. Kaushik, H. Garg, M. Singh, and B. Prasad, "Advancement and challenges in MOSFET scaling," *Materials Science in Semiconductor Processing,* vol. 134, p. 106002, 2021.

[8] A. Shilov, "TSMC: First 7nm EUV Chips Taped Out, 5nm Risk Production in Q2 2019," *AnandTech, October,* vol. 9, 2018.

[9] A. Shilov, "Samsung completes development of 5nm EUV process technology," *URL: https://www. anandtech. com/show/14231/samsung-completesdevelopment-of-5-nm-euv-process-technology (дата обращения: 7.03. 2020),* 2019.

[10] H. Sood, V. M. Srivastava, and G. Singh, "Advanced MOSFET Technologies for Next Generation Communication Systems-Perspective and Challenges: A Review," *Journal of Engineering Science & Technology Review,* vol. 11, no. 3, 2018.

[11] G. G. Shahidi, "Challenges of CMOS scaling at below 0.1/spl mu/m," in *ICM 2000. Proceedings of the 12th International Conference on Microelectronics.(IEEE Cat. No. 00EX453)*, 2000: IEEE, pp. 5-8.

[12] L. Wilson, "International technology roadmap for semiconductors (ITRS)," *Semiconductor Industry Association,* vol. 1, 2013.

[13] A. Mahmood and K. Gaeid, "Review and Case Study on Control of Induction Motor Using High-Level Converter," *Anbar Journal of Engineering Science,* vol. 15, no. 1, pp. 41-53, 2024.

[14] J. Qu, H. Zhang, X. Xu, and S. Qin, "Study of drain induced barrier lowering (DIBL) effect for strained Si nMOSFET," *Procedia Engineering,* vol. 16, pp. 298-305, 2011.

[15] A. Wagadre and S. Mane, "Design & performance analysis of DG-MOSFET for reduction of Short Channel effect over bulk MOSFET at 20nm," *International Journal of Engineering Research and Applications,* vol. 4, no. 7, pp. 30-34, 2014.

[16] C. Alexander and A. Asenov, "Statistical MOSFET current variation due to variation in surface roughness scattering," in *2011 International Conference on Simulation of Semiconductor Processes and Devices*, 2011: IEEE, pp. 275-278.

[17] I. Saad, M. L. Tan, M. T. Ahmadi, R. Ismail, and V. K. Arora, "The dependence of saturation velocity on temperature, inversion charge and electric field in a nanoscale MOSFET," *Int. J. Nanoelectronics and Materials,* vol. 3, pp. 17-34, 2010.

[18] S. Chaudhary, B. Dewan, C. Sahu, and M. Yadav, "Steep-subthreshold slope dual gate negative capacitance junction less FET with dead channel: TCAD approach for digital/RF applications," *Microelectron J,* vol. 127, p. 105518, 2022.

[19] J.-W. Han, C.-H. Lee, D. Park, and Y.-K. Choi, "Quasi 3-D velocity saturation model for multiple-gate MOSFETs," *IEEE transactions on electron devices,* vol. 54, no. 5, pp. 1165-1170, 2007.

[20] G. A. Gauhar, A. Chenchety, H. Yenugula, V. Georgiev, A. Asenov, and O. Badami, "Study of gate current in advanced MOS architectures," *Solid-State Electronics,* vol. 194, p. 108345, 2022.

[21] W. M. Zapar, K. Gaeid, H. B. Mokhlis, and T. A. Al Smadi, "Review of the most recent articles in fault tolerant control of power plants 2018–2022," *Tikrit Journal of Engineering Sciences,* vol. 30, no. 2, pp. 103-113, 2023.

[22] A. Godoy, J. López-Villanueva, J. Jiménez-Tejada, A. Palma, and F. Gámiz, "A simple subthreshold swing model for short channel MOSFETs," *Solid-State Electronics,* vol. 45, no. 3, pp. 391-397, 2001.

[23] R. W. Kelsall, I. W. Hamley, and M. Geoghegan, "Nanoscale Science and Technology," 2005.

[24] R. D. Clark, "Emerging applications for high K materials in VLSI technology," *Materials,* vol. 7, no. 4, pp. 2913-2944, 2014.

[25] D. Rairigh, "Limits of CMOS technology scaling and technologies beyond-CMOS," *Institute of Electrical and Electronics Engineers, Inc,* 2005.

[26] H. L. Lu and D. W. Zhang, "Issues in high-k gate dielectrics and its stack interfaces," *High-k Gate Dielectrics for CMOS Technology,* pp. 31-59, 2012.

[27] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Materials Science and Engineering: R: Reports,* vol. 88, pp. 1-41, 2015.

[28] G. Wilk, "High-k gate dielectrics: Current status and materials properties condiderations," *J. Appl. Phys,* vol. 89, no. 10, pp. 5423-5275, 2001.

[29] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process-variation effect, metal-gate work-function fluctuation, and random-dopant fluctuation in emerging CMOS technologies," *IEEE Transactions on Electron Devices,* vol. 57, no. 2, pp. 437-447, 2009.

[30] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE,* vol. 89, no. 3, pp. 259-288, 2001.

[31] C.-H. Choi, P. Chidambaram, R. Khamankar, C. F. Machala, Z. Yu, and R. W. Dutton, "Dopant profile and gate geometric effects on polysilicon gate depletion in scaled MOS," *IEEE Transactions on Electron Devices,* vol. 49, no. 7, pp. 1227-1231, 2002.

[32] R. K. Ratnesh *et al.*, "Advancement and challenges in MOSFET scaling," *Materials Science in Semiconductor Processing,* vol. 134, 2021, doi: 10.1016/j.mssp.2021.106002.

[33] P. M. Zeitzoff, "MOSFET Scaling Trends, Challenges, and Key Associated Metrology Issues Through the End of the Roadmap," presented at the AIP Conference Proceedings, 2005.

[34] T. Sakurai, A. Matsuzawa, and T. Douseki, *Fully-depleted SOI CMOS circuits and technology*. Springer, 2006.

[35] R. Simonton, "Special report: SOI wafer technology for CMOS ICs," *Robert Simonton, President Simonton Associates,* pp. 1-11, 2002.

[36] M. K. Anvarifard and Z. Ramezani, "A novel nanoscale FD-SOI MOSFET with energy barrier and heat-sink engineering for enhanced electric field uniformity," *Micro and Nanostructures,* vol. 196, p. 207986, 2024.

[37] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge university press, 2003.
[38] S. Kundu and J. K. Mandal, "Design and analysis of logic circuits based on 8 nm double gate MOSFET," *Microsystem Technologies,* pp. 1-18, 2024.
[39] M. M. Manjula and R. Ramesh, "Performance analysis of MoTe2/MoSe2 and MoTe2/WSe2 heterostructure double-gate MOSFET," *J Electron Mater,* vol. 52, no. 11, pp. 7694-7707, 2023.
[40] Q. Wang, H. Liu, S. Wang, and S. Chen, "TCAD simulation of single-event-transient effects in L-shaped channel tunneling field-effect transistors," *IEEE Transactions on Nuclear Science,* vol. 65, no. 8, pp. 2250-2259, 2018.
[41] A. Khaliq and S. Zhang, "Doping engineering to enhance the performance of double-gate p MOSFETs with ultrashort gate length (5 nm)," *Journal of Computational Electronics,* vol. 20, no. 3, pp. 1178-1186, 2021.
[42] S. Tiwari and R. Saha, "Methods to reduce ambipolar current of various TFET structures: a review," *Silicon,* vol. 14, no. 12, pp. 6507-6515, 2022.
[43] J. Madan and R. Chaujar, "Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability," *IEEE Transactions on Device and Materials Reliability,* vol. 16, no. 2, pp. 227-234, 2016.
[44] S. L. Moskowitz, *Advanced materials innovation: Managing global technology in the 21st century*. John Wiley & Sons, 2016.
[45] D. Peftitsis and J. Rabkowski, "Gate and Base Drivers for Silicon Carbide Power Transistors: An Overview," *IEEE Transactions on Power Electronics,* pp. 1-1, 2015, doi: 10.1109/tpel.2015.2510425.
[46] R. K. Ratnesh and M. S. Mehata, "Controlled synthesis and optical properties of tunable CdSe quantum dots and effect of pH," *AIP Advances,* vol. 5, no. 9, 2015, doi: 10.1063/1.4930586.
[47] C. Yalung, W. Yamwong, and D. Tantraviwat, "Optimization of Multi-fins FinFET Implemented on SOI Wafer Based on SiGe and Gaussian Process Regression," *IEEE Access,* 2024.
[48] R. R. Das, T. Rajalekshmi, and A. James, "FinFET to GAA MBCFET: a review and insights," *IEEE Access,* vol. 12, pp. 50556-50577, 2024.
[49] A. J. Butrica, "NASA's Role in the Manufacture of Integrated Circuits," *Historical Studies in the Societal Impact of Spaceflight. Washington: National Aeronautics and Space Administration,* 2015.
[50] R. K. Bassett, *To the digital age: Research labs, start-up companies, and the rise of MOS technology*. JHU Press, 2003.
[51] Y. Kuo, "Thin film transistor technology—Past, present, and future," *The Electrochemical Society Interface,* vol. 22, no. 1, p. 55, 2013.
[52] M. S. Kim *et al.*, "Statistical analysis of increased immunity to poly-si grain boundaries in nanosheet CMOS logic inverter through sheet stacking," *Silicon,* vol. 16, no. 16, pp. 5855-5864, 2024.
[53] R. R. Das, T. Rajalekshmi, and A. James, "FinFET to GAA MBCFET: a review and insights," *IEEE Access,* 2024.
[54] M. Lundstrom, "Is nanoelectronics the future of microelectronics?," in *Proceedings of the 2002 international symposium on Low power electronics and design*, 2002, pp. 172-177.
[55] J. Appenzeller, "Carbon nanotubes for high-performance electronics—Progress and prospect," *Proceedings of the IEEE,* vol. 96, no. 2, pp. 201-211, 2008.
[56] M. Elangovan and K. Gunavathi, "Effect of CNTFET parameters on novel high stable and low power: 8T CNTFET SRAM cell," *Transactions on Electrical and Electronic Materials,* vol. 23, no. 3, pp. 272-287, 2022.
[57] A. S. Al-Jawadi, M. T. Yaseen, and Q. T. Algwari, "Gate engineering solutions to mitigate short channel effects in a 20 nm MOSFET," *e-Prime - Advances in Electrical Engineering, Electronics and Energy,* vol. 11, 2025, doi: 10.1016/j.prime.2025.100934.