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# Design of RF Power Amplifier Techniques for 5G and Beyond Communication Systems: A Review

Ahmad A. Ismael[a], Mohammad Tariq Yaseen[b,c]
[a] *Department of Electrical Engineering, Collage of Engineering, University of Mosul, Mosul, Iraq*
*Email: a.a.ismail@uomosul.edu.iq ; ORCID: https://orcid.org/ 0009-0003-4570-6146*
[b] *Department of Electrical Engineering, Collage of Engineering, University of Mosul, Mosul, Iraq*
*Email: mtyaseen@uomosul.edu.iq ; ORCID: https://orcid.org/0000-0001-7173-8684*
[c] *Department of Communications and Intelligent Digital Systems Engineering, University of Mosul, Mosul, Iraq*
*Email: mtyaseen@uomosul.edu.iq ; ORCID: https://orcid.org/0000-0001-7173-8684*

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**ABSTRACT**

This review article discussed power amplifiers in modern wireless transmission systems, clarifying the determinants and restrictions of the create of power amplifiers in 5G and beyond transmission systems. The important topics of power amplifier design were discussed, which included solid-state techniques contributing to building the basic building block of the amplifier, furthermore to techniques for building the electronic circuit topology, while clarifying the importance of techniques for improving efficiency and linearity. This paper contributed to highlighting optimization and manufacturing techniques, focusing on the determinants and advantages of each technology. And clarifying the research space for researchers with the aim of developing a power amplifier that is optimal for use in modern wireless communications systems.

## 1. Introduction

Today, the world's communications industry is undergoing a massive transformation, as this kind of communication's forms and purposes have expanded. Wireless communication systems and mobile phones, as an example, have developed over the last decades, and smart systems have emerged as a result. Nowadays, the use of communications system is going beyond just telephone communication; they can also be used in global positioning system, data and image transmission, satellite communication, and remote control over the internet [1-5]. Consequently, there was a pressing need to create communications infrastructure and satisfy the growing demands for more capacity and maximum transmitted data rate. So the fifth generation of communications has emerged to provide a wireless network everywhere to achieve new services through the rapid and highly reliable transmission of data [6-8]. Current applications of communication systems impose difficult requirements on the wireless system, and to achieve acceptable system performance, special attention must be given to the design of the circuit topology and system engineering. In the transmitter, power amplifiers must process complex modulated signals,

* Corresponding author: Mohammad Tariq Yaseen; mtyaseen@uomosul.edu.iq ; +964-7736977178

characterized by a high peak-to-average power ratio (PAPR) and a wide modulation bandwidth. Furthermore, power amplifiers must maintain high efficiency to reduce power consumption and mitigate thermal cooling issues [9-11].

The power amplifier operates by integrating its components, which consist of the transistor as the fundamental unit of the amplifier, along with the matching circuits at both the input and output. These parts work together to achieve an appropriate amplification of the information signal with an appropriate power and linearity that is sent to the antenna, which in turn sends the signal through the transmission channel[12],[13].This paper includes a review of the power amplifier architectures used in modern communications systems, along with the techniques used to improve the performance of the power amplifier, in addition to presenting the most important electronic device manufacturing techniques used in building the basic amplification unit, which is the transistor. These issues have been discussed collectively, clarifying their impact on the performance of the power amplifier, so that this paper serves as a summary of many important and recent works to assist researchers working in this field.

The structure of the paper is as follows. The second section deals with presenting solid state devices technologies for power amplifiers with a summary of the results of a group of research that dealt with this topic. The third section will present examples of power amplifier circuit topologies that efficiently and linearly amplify wide dynamic range signals. While, techniques for improving efficiency and linearity father more power combining techniques were covered in the fourth section. Finally, the conclusion is discussed in Fifth section followed by references.

## 2. Solid-State Technologies

The Device technologies adopted in the PA design have great importance to the overall power output. This is because the power produced never relies on the electronic amplifier circuit only. Rather, it depends mainly on the power density of the transistor technology. Another important point is the amplification characteristics of the working region, i.e. the frequency at which the transistor operates, so that the amplifier can amplify the power at that frequency. That is, the amplifier gives the appropriate amplification at the required power at the appropriate frequency [14-20] . One of the important elements by which the effectiveness of the amplifier is evaluated is the output power, which be determined by the power density produced per unit volume, which varies between the types of technologies that manufacture electronic devices. Another important element is the power gain in the working area, which is directly determined by the cut-off frequency (fT) in addition to the maximum frequency ($f_{MAX}$) [21]. An example of this is MOSFET technology.

$$f_T = \frac{g_m}{2\pi\sqrt{{C_{gs}}^2 + 2C_{gs}C_{gd}}} \quad (1)$$

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \quad (2)$$

Where gm is transconductance, Cgs, Cgd, are transistor parasitic capacitor Rg is the parasitic gate resistance[21],[22]. The frequency performance of the amplifier, which determines the linear characteristics of the amplifier, is inversely proportional to the equivalent capacitance, which depends mainly on the effective area of the device, as shown in Equation 1 and Equation 2. Unfortunately, the output power depends directly on the effective area, so efficiency and linearity are traded off at the transistor level. However, if you look separately, linearity is severely related to the transistor property, such as the transconductance profile, the dynamic non-linearity, the existence of traps. Furthermore, other transistor features, such as the ratio of knee voltage to drain bias, can have an effect on efficiency.

The previous considerations clearly reflect the characteristics of the different types of technologies. Fig 1. shows the difference in maximum output power as in relation of frequency, for different technologies, where (CaN) takes the lead in power production, while (CMOS) technology appears to produce the least power, while all technologies share a decrease in power with increasing frequency. This is due to the effect of parasitic capacitors, which are less effective in the indium phosphide (InP) technique. Therefore, we notice an extension of the response to higher frequencies than in the rest of the techniques [23-27]. The response to each technique is represented by a specific colour, but the response parameter is represented by a straight line in the same colour.

An example of study in this field is the device being tested, 0.5 micrometre gate length (LG) AlGaN/GaN HEMT on silicon. TCAD simulation

recreates the structure and device geometry, whereas ATHENA was used to achieve the process flow [25]. A scheme with two dimensions is described in Fig 2.

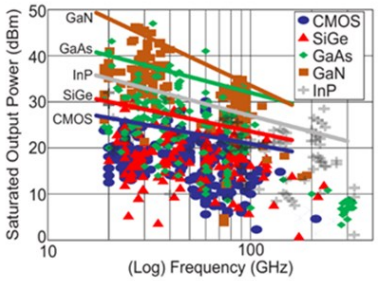


**Figure 1.** The characteristics of different types of technologies in the range from K-band to over 300 GHz[25].

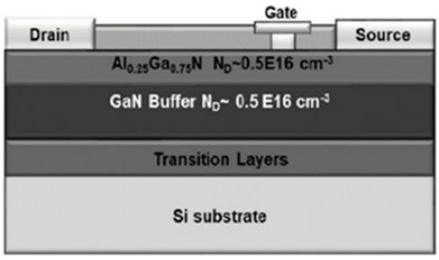


**Figure 2.** The Structure of AlGaN/GaN HEMT at the test [28].

Table 1. displays the results of a group of researches which focused on transistor technologies and comparing these results in terms of power density, maximum frequency, and breakdown voltage. The results showed the different capabilities of these techniques. The designer or researcher can choose the appropriate technology for the design to obtain appropriate power at a specific frequency. Then the response of the amplifier is improved in terms of linearity, output power, breakdown voltage, and amplifier size by controlling the dimensions of the transistor.

## 3. Power Amplifier Circuits Techniques

The successful operation of a power amplifier is not predominantly influenced by the type of transistor employed, but rather by the other components of the amplifier, including the electronic circuit topology and the input and output matching circuits, which are essential for attaining optimal compatibility with system requirements. The researchers are worked on these circuits to improve frequency response, transfer characteristics, and amplifier stability, thereby contributing to high performance and enhanced signal quality[27],[37-39].

The function of the power amplifier is to boost the signal with appropriate linearity and efficiency to make the communication process successful. The power amplifier is frequently changing and developing with the development of communications systems. In the analog generation of communications system, traditional amplifiers or bias amplifiers are used to amplify the information signal. Reliance on these types of amplifiers continued until the first generations of digital systems with a constant envelop signal appeared. However, with the advancement of communications systems, in the third generation and the following, with the beginning of non-constant envelop signal systems, it became important to operate amplifiers in variable power ranges due to the change in the modulated signal over a wide power range. Therefore, there was a need to expand the dynamic range of the amplifier (DR), in addition to increasing the efficiency of the amplifier in the low power region Back off power (BOP). To achieve this, a suitable power amplifier architecture was proposed to improve efficiency, increase output power with high linearity, so switch mode power amplifiers were the appropriate solution. The major turning point in communications systems occurred after the emergence of the Internet of Things (IOT) and the need to connect things to the Internet, including

**Table 1.** Process Configuration for Different Transistor Technologies

| Technology | Gate length/Emitter width (nm) | Power density (mW/mm) | fT (GHz) | fMAX (GHz) | GD/CE Breakdown (V) | Ref. |
|---|---|---|---|---|---|---|
| GaAs pHEMT | 150 | 560–1000 | 70–85 | 120 | 12–16 | [29] |
| InP HBT/DHBT | 256–250 | 500 | 375–520 | 650–850 | 4 | [30,31] |
| SiGe BT/BiCMOS | 130–120 | - | 200–270 | 260–450 | 1.6–3.5 | [32] |
| GaN/Si HEMT | 100 | 3300–4000 | 100 | 180 | 25–50 | [33] |
| GaN/SiC HEMT | 40 (T3) | 300 | 200 | 400 | 40 | [34] |
| Si CMOS/SOI | 45 | 50 | 300–400 | 350–500 | - | [35], [36] |

self-driving vehicles, measuring devices, and monitoring systems, in addition to the demand to expand the traditional communications network (and increase the number of subscribers) and the need to transfer a large amount of data. To realize this, the Transmission Band-width must be increased with the frequency of the carrier wave of the information signal of the communication system. To guarantee the success of the communication process in this system, it was essential to construct a power amplifier that fulfils these specifications. Thus, these requirements ware translated into specifications and limitations that pose real difficulties for power amplifier designers. Table 2. below illustrates the amount of challenges that the power amplifier faces with the advancement of successive generations of communications [40-43].

**Table 2.** Characteristics of digital communications systems for successive generations [44-48].

| Generation | 3G | 4G | 5G |
|---|---|---|---|
| Technology | WCDMA | LTE | 5G NR |
| Access Protocol | CDMA | OFDMA | OFDMA/BDMA |
| Frequency GHz | 0.9 - 2.6 | 0.9 - 2.6 | sub-6 / 24-40 |
| Bandwidth MHz | 3.84 | 20 | >100 |
| Data Rate | 2Mbps | 1Gbps | 10Gbps |
| PAPR dBm | >6 | <10 | >12 |

Power amplifiers in 5G systems and beyond face major challenges in achieving the desired goal of signal amplification due to the signal requirements in terms of linearity, bandwidth and efficiency. Table 2, shows that the frequency at which the amplifier operates in the fifth generation is higher compared to previous generations. This means that the parasitic elements of the transistor will be more effective compared to previous generations. The Table 2, also shows an increase in data rate for 5G system with high data rate need modulated signal with high bandwidth and large peak to average power ratio of modulated signal which in turn requires wide bandwidth in addition to high (DR) for the amplifier, and this in turn imposes high linearity for the amplifier and constant gain over a wide range of changing the output power[42] . Fig 3. clearly shows this fact.

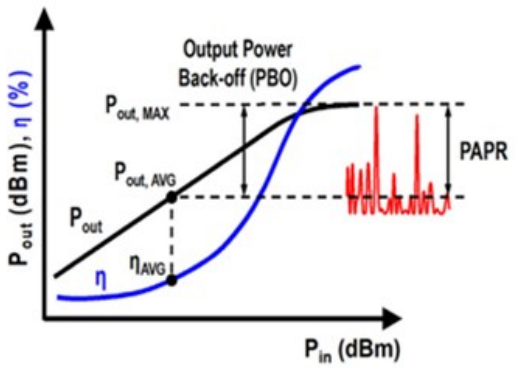


**Figure 3.** Output power and efficiency vs. input power under the presence of a modulated signal with high PAPR [1]

The application of fifth generation technology apply to achieve the (IOT) service, presence of (MIMO) technology, in addition to the presence of autonomous vehicles, imposes on the amplifier the technology of controlling the output power to send the power to different ranges and in a specific direction directive antenna need, and this is done using power combiner technology. Power combiner technology is essential to achieving these goals, and this in turn comes at the expense of complicating the amplifier circuit. The transistor technology is often imposed on the designer for several reasons, including the cost of manufacturing or the available technology, and sometimes the requirements of the system to be used force the use of a specific technology. These technologies are another important limitation that must be taken into consideration, because electronic device technology determine the power density, maximum frequency, and parasitic elements, in addition to the maximum voltage that the transistor can carry. All of these challenges together must be dealt with and we have to compromise between them to achieve the optimal design of the power amplifier by obtaining an appropriate solution at the electronic circuit level that suits use in a specific application.

Based on the above, many techniques for fabricating, constructing, structuring, shaping electronic circuits for power amplifiers were discussed, which were covered by a group of researchers to be the focus of presentation and analysis to serve as a foundation for designing

power amplifier in fifth generation and beyond. They were arranged according to the following sections approaches:

### *3.1. Switch Mode Power Amplifier*

In power amplifiers, especially at high frequencies, reliance is placed on reducing the current conduction angle to obtain an effective balance between efficiency and linearity. Conventional amplifier types such as (Class AB, B) are suitable for this type of application, but the main problem that these amplifiers suffer from is high power losses. Inside the transistor. Therefore, the load circuit was developed to form the voltage and current wave at the transistor output so that the interference between the voltage wave and the current was as little as possible, and this idea was realized with the emergence of switched mode power amplifiers. Fig 4. shows the basic circuit of the switch power amplifier and the structure of both the current and voltage waves.

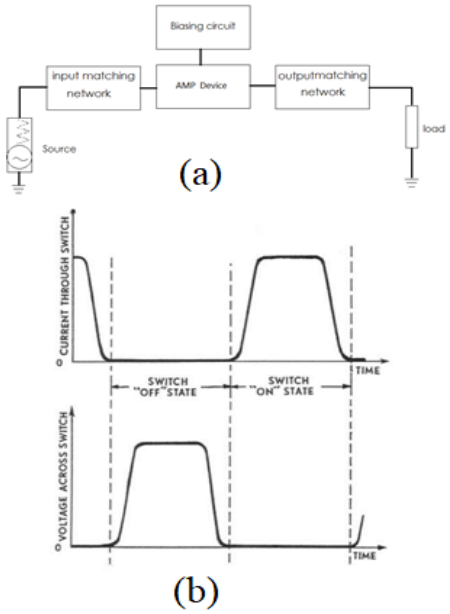


**Figure 4.** (a)General construction of a switched mode power amplifier, (b) Conceptual Target Waveform[37],[49].

Despite the efficiency of switched technique power amplifiers, they suffer from low linearity due to the direct effect of parasitic capacitors on the wave shaping circuit, thus limiting their operation at high frequencies. In addition to the above, there is the problem of needing a transistor that can handle a high voltage equal to at least twice the power supply voltage, and this problem is more severe with the need to increase the frequency because increasing the frequency requires reducing the dimensions of the device and thus reducing the power and breakdown voltage of the transistor. There are many studies that address the design of power amplifiers and overcoming the challenges facing designers in such amplifiers. This paper discusses a group of these studies.

Class E switched mode power amplifier was used in IoT wireless communication application with suitable bandwidth[50]. The linearity of the amplifier was improved using cross coupling neutralization technique. Through this technique, the effect of the Cgs capacitor was reduced, and better reverses isolation was obtained. Furthermore, by using the differential topology, the output voltage was doubled and high-power gain is obtained. At 2.4 GHz, the designed amplifier produces 29.5-dBm output power with 45% DE and 43.5% PAE.

The research [10], dealt with improving the response of the power amplifier in conditions of efficiency and linearity. The wave shaping circuit using a type Y amplifier had a significant impact in improving efficiency, and the wave trap circuit in the output circuit using a Class F load circuit was important in improving linearity and reducing the effect of parasitic elements at high frequencies, Thus, at an output power of 21 dBm, the simulated amplifier achieved a gain of 26 dB and a power added efficiency of 51%. The corresponding reductions for second and third harmonic components were -47.6 dBc and -79.3 dBc.

The theoretical introduction and practical validation of the Continuous Class F Mode Power Amplifier, which opens up a new design area for the creation of wide-band and highly efficient power amplifiers, are presented in another work This work demonstrates that connected fluctuations of fundamental and second harmonic impedances may be maintained at constant or even higher output power and efficiency. The study, which was conducted on GaAs PHEMT devices, shows that throughout a broad range of fundamental and second harmonic loads, a nearly constant efficiency between 82% and 87% can be attained coupled with a flat output power of 20dBm[11].

In paper research[12], the problem of high voltages was addressed which collapse of the

transistor under the influence of increased voltages as a result of the formation of voltage waves shaping by taking advantage of the characteristics of CaN Technology in withstanding voltages. The use of a two-stage amplifier greatly increased the gain. Linearity was improved and the amplifier's bandwidth was increased through the matching circuit for the two stages of the amplifier. In addition to the linearity effects resulting from the stability and consistency of the amplifier's gain for a wide range of output power.

Table 3 juxtaposes the findings of many research investigations concerning the design of switched mode power amplifiers utilizing different types of transistors. It illustrates the variance in outcomes attributable to distinct methodologies.

### *3.2. Cascode Power Amplifier*

The Miller effect in power amplifiers refers to the apparent increase in input capacitance CM due to the feedback capacitance between the output and input terminals, such as the gate-drain capacitance (Cgd). This effect becomes more significant at high frequencies, as it limits bandwidth and slows down the amplifier by forming a low-pass filter. To minimize the Miller effect, designers often use cascode configurations, which reduce the gain across (Cgd)

$$CM=Cgd(1+Av) \quad (3)$$

Using the Cascade Technique, connecting common-source (CS) and common-gate (CG) transistors are connected in series, as depicted in Fig 5. This configuration is commonly utilized in power amplifier (PA) designs to increase both bandwidth and gain[19].The cascode structure offers several benefits, including increased reverse isolation, high output impedance and reduced sensitivity to change transistor output resistance. The minimal Miller feedback capacitance is responsible for the improved reverse isolation [53-56]. In the cascode configurations, the small signal voltage open loop gain is defined as [19].

$$A_{vo}=\frac{V_o}{V_i}=-g_{m1}r_{o1}\times(1+g_{m2}r_{o2})$$

$$\approx -g_{m1}r_{o1}g_{m2}r_{o2}\approx -g_m^2r_o^2 \quad (4)$$

the parameters $gm$ and $ro$ represent the transconductance gain and transistor output impedance, respectively. Numerous research studies have addressed this topic, using the characteristics of this amplifier to build amplifiers suitable for use in the fifth generation and beyond. A number of these studies are presented to shed light on the key aspects that have contributed to improving the amplifier's performance.

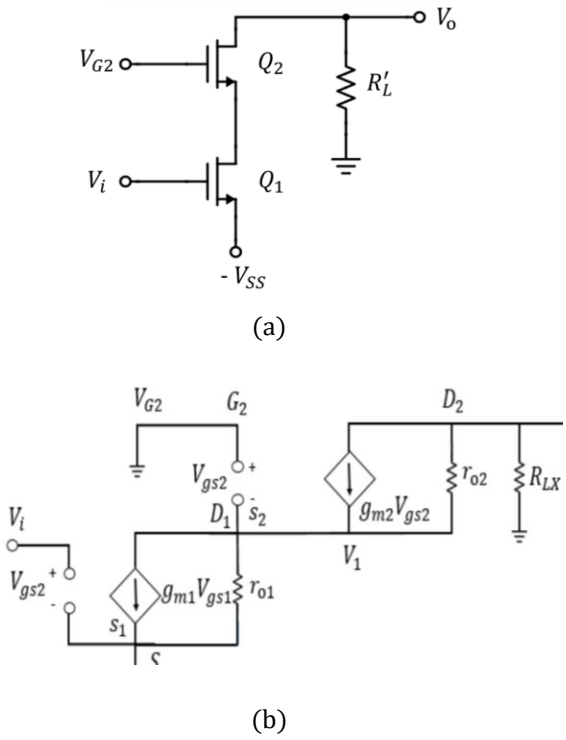


**Figure 5.** Cascode PA configuration (a) schematic diagram and (b) small signal equivalent circuit[54].

The paper research addresses the limitation of traditional cascode amplifiers in achieving fast settling times, which are essential in high-speed

**Table 3**. Results of a group of research that deliberate on switched power amplifiers

| Ref | Technology | Psat (dBm) | PAE % | Freq GHz | Gain dB | BW MHz | Applications | VDD (v) | Class of Operation |
|---|---|---|---|---|---|---|---|---|---|
| [50] | 0.18 µm CMOS | 29.5 | 43.5 | 2.4 | 36 | 1 | IoT | 1.8 | Class-E |
| [51] | 65nm CMOS | 21 | 51 | 5 | 26 | 1 | 5G | 2.5 | Class-EF |
| [52] | 0.25-µm GaN | 39.1 | 50.9 | 5 | 20.4 | 100 | 5G NR n79 | 28 | Class-F |

applications. To overcome this issue, the researchers proposed an improved cascode structure with a fully differential design to enhance efficiency and performance [57]. Another problem addressed in research [58] was the challenge of designing efficient power amplifiers at millimeter-wave frequencies like 28 GHz, where parasitic effects and voltage stress can severely impact performance. The authors tackled this obstacle by introducing a switched-cascode Class E amplifier implemented in 22 nm CMOS FDSOI technology, which combines cascode protection with efficient switching to handle high voltages and improve performance. The results showed that the amplifier achieved high output power and good efficiency at 28 GHz, demonstrating the viability of the switched-cascode approach for millimetre-wave applications.

The difficulty of using cascode and regulated cascode stages in ultra-low-voltage (ULV) circuits was addressed, where traditional designs face headroom limitations in this field. The authors investigated the behaviour of these amplifier stages when operating MOSFETs in the deep subthreshold region, analysing both theoretical models and experimental results. The research concluded that regulated cascode stages are feasible in ULV environments if careful attention is paid to device sizing and biasing, allowing acceptable performance even at very low supply voltages [59]. In the field of optical communication systems, two studies have addressed this issue. The first one tackles the common problem of limited gain bandwidth output and high power consumption in Transimpedance Amplifiers (TIA), which are essential in applications such as optical receivers. The researchers proposed using a cascade amplifier with local feedback to stabilize the gain and improve input impedance while reducing voltage margin requirements[60]. The issue of achieving high gain and wide bandwidth while preserving low power loss in Operational Transconductance Amplifiers (OTAs) was handled in the second study [61]. The researchers proposed folded cascode OTAs with interleaved local feedback techniques and adaptive biasing to optimize power usage based on signal conditions. The results display that the proposed amplifier achieved a significant effect in DC gain, broad bandwidth, and high-power efficiency compared to traditional folded cascade designs.

### *3.3. Distributed Power Amplifier*

Distributed power amplifiers (DPAs) combine conventional amplifier circuit design with transmission line principles to achieve a high-gain, wide-bandwidth amplifier. This concept, pioneered by Percival in 1937and called a distributed power amplifier. The effect of parasitic capacitors connected to the drain and gate of a transistor is reduced by the transmission lines, improving the amplifier's bandwidth. Also known as traveling-wave amplifiers, distributed power amplifiers (DPAs) use input and output transmission lines connected to multiple active cells, usually transistors, often microchip lines. As the input signal propagates through the gate line, each transistor responds by generating a complementary waveform on the drain line, producing phase-summed output signals. Unlike cascaded active cells with double gain, distributed power amplifiers have summed gain characteristics. Terminating the input and output transmission lines with Zg and Zd reduces reflections, and Fig 6. shows the construction of this type of amplifier [62-64].

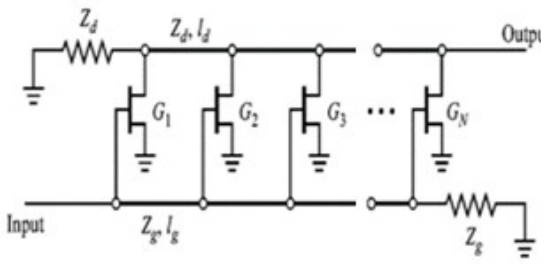


**Figure 6.** shows the installation of DA with N stage[62].

The research paper [63] addresses the creation and execution of a CMOS distributed power amplifier (DA) operating across a wide frequency range. The problem involves achieving high-performance amplification across a broad spectrum while mitigating the effects of parasitic capacitances in transistors. The method employed involves utilizing combined transmission lines to absorb these parasitic capacitances, enhancing the amplifier's bandwidth. The results show successful amplification from 2 to 22 GHz, showcasing improved linearity and efficiency compared to traditional designs. Another study [62] challenges the challenge of designing a power amplifier capable of reaching a high power gain. The problem

involves addressing the compromise between power gain and linearity, which is critical in high-performance amplifier design. The technique of treatment involves employing a distributed architecture, distributing the amplification task across multiple amplifier modules to reduce issues like gain compression and nonlinearity. Additionally, careful optimization of the amplifier's components and interconnections is conducted to maximize power gain while preserving linearity. The results indicate that the distributed power amplifier designed by Tanique has advantages, as it produces a significant increase in power gain without sacrificing linearity when compared to congenital single-stage amplifiers. The goal of the study [64] is to develop high efficiency wide band power amplifier utilizing 130 nm CMOS technology. Achieving wide frequency coverage while reducing power consumption and guaranteeing linear performance is the difficult part. Using stacked distributed architecture with a uniform distributed topology is the strategy used. This strategy spreads the amplification task across multiple stages to improve both bandwidth and efficiency. In order to optimize overall performance, the CMOS implementation is also sensibly optimized. The results indicate that the wide band power amplifier was successfully realized, with improvement in bandwidth and efficiency above previous designs in the same filed of technology.

### *3.4. Stacked Power Amplifier*

A common method for increasing the allowable supply voltage range in CMOS technology is used the cascode or stacked transistor topology. this arrangement maintains high reliability standard and allows operation at elevated supply voltages when associated with thick-oxide transistor. This yields increased output power, enhanced load capacity, and reduced current, potentially resulting in diminished losses and heightened efficiency. Moreover, the output impedance is elevated compared to a single common-source stage. The typical configuration is illustrated in Fig 7. In this setup, the lower transistor, M1, functions in a common-source configuration, being propelled by the input signal. Meanwhile, the upper transistor, M2, is typically linked to the supply voltage. M2 operates in common gate mode (with the gate grounded) at high frequencies due to the presence of an additional capacitor $C_{LARGE}$.

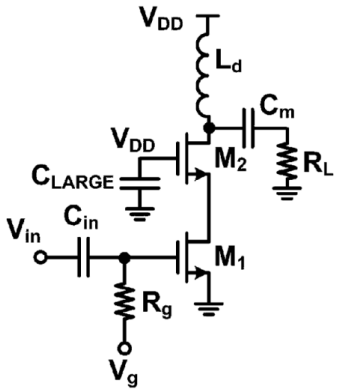


**Figure 7.** The stacked transistor structure of power amplifier [65].

Many studies on this topic have led to the creation of power amplifier for advanced digital communications systems. Among these research and studies The thesis[66], which addresses the challenge of enhancing power amplification in millimetre wave (MM-wave) frequencies utilizing MOS (Metal-Oxide-Semiconductor) technology. The primary focus is on investigating the feasibility and effectiveness of stacked MOS configurations to achieve higher output power, improved load capacity, and reduced current consumption while maintaining reliability.

The research paper addresses the issue of developing a power amplifier operating at 28 GHz. Specifically, a Symmetrical Doherty architecture using stacked-FET cells is used [67]. At millimetre-wave frequencies, where traditional power amplifier design is constrained, the main challenge is to produce high efficiency power amplification. The process of treatment demands designing a Symmetrical Doherty power amplifier, which is recognized for its efficiency enhancement method, coupled with stacked-FET cells to further improvement power handling capabilities. Through a combination of circuit simulations, layout optimizations, and performance estimates the research shows the efficiency of the proposed approach. The results indicate notable gain in efficiency and power handling over conventional designs, which makes the amplifier suitable for 28 GHz applications like a radar or 5G communication systems.

In the study [71], the challenge of designing a power amplifier able to function over a broad frequency band (57 to 85 GHz) while delivering

high output power (18 dBm) is discussed. The main problem is to circumvent constrains of CMOS technology at such high frequencies and achieve both wide band performance and high power output. The treatment strategy makes use of a 4-stack FET (Field-Effect Transistor) configuration realized using a 45-nm Silicon-On-Insulator (SOI) CMOS technology. The research shows the success of the suggest approach through meticulous characterization, optimization technique, and careful circuit design. The results illustrate that the power amplifier achieves the desired output power level across the given frequency range while maintaining acceptable levels of efficiency and linearity. This represents an important advancement in millimetre-wave CMOS power amplifiers, with possible uses in fields like applications in areas such as wireless communication, radar systems, and sensing technologies. Main difficulty lies in creating power amplifiers that can function essentially at millimetre-wave frequencies and offer high output power with efficiency.

The use of a triple-well technique with a multi-stacked CMOS design is suggested in the paper stages[76]. To control high voltage and produce more power, this method builds many stacked transistors. It also makes use of the triple-well technique to enhance isolation and reduce substrate noise, both of which are essential at high frequencies. The findings demonstrate that, within the intended millimetre-wave frequency range, multi-stacked CMOS power amplifiers designed using the triple-well process demonstrate notable gains in output power, efficiency, and performance stability, rendering them appropriate for phased array applications like advanced radar systems and 5G communications. Table.4, summarizes the results of a group of research studies that used different methods to improve the performance of the amplifier at the electronic circuit level and show the impact of different technologies on the amplifier's operating frequency, bandwidth, output power, and operating voltage is observed.

## 4. Enhancement Power Amp Performance Techniques

There are many techniques used to improve the performance of the power amplifier, and the purpose of these techniques is to enhance the amplifier's performance. These techniques are used to enhance the amplifier's response to meet the system's necessities for linearity, efficiency, and output power, which the design has reached its maximum limits at the transistor level and the electronic circuit level. The diversity and differences of these technologies are due to the varying requirements of communication systems and their applications, where the appropriate enhancement technology is chosen based on the

**Table 4.** Summarizes the results of several studies that employed various techniques

| Ref | Technology | Circuits Techniques | Topology | Freq GHz | BW GHz | Output Power dBm | PAE (%) | Gain dB | Application |
|---|---|---|---|---|---|---|---|---|---|
| [68] | GaN HEMT | Switching modes | Class-E | 3.8 | 1.3 | 41.6 | 74.2 | 11.6 | 5 G |
| [69] | GaN HEMT | Switching modes | Class-F | 4.3 | 1 | 41.32 | 79.9 | 11.3 | 5G |
| [70] | GaN | Switching modes | Class-EF | 3 | 1.5 | 41.4 | 70 | 15 | 5G |
| [56] | GaN | Cascode | tandem-cascade | 20 | 30 | 30 | 33 | 9.6 | high power |
| [58] | CMOS FDSOI | Cascode | compound | 28 | - | 13 | 28 | 8.5 | sub mm-W |
| [71] | CMOS | Cascode | Bias Controls | 1.85 | - | 27.7 | 46.2 | 27.2 | RF |
| [63] | CMOS | Distributed | compact | 2–22 | 20 | 14.5 | 10 | 11.9 | Radar system |
| [62] | GaN | Distributed | tapering technique | 3.4 | DC-3.4 | 41.6 | 27 | 22 | RF |
| [72] | InP | Distributed | nine-stage DA | 115 | 7-115 | 24 | 6.8 | 16 | mm-W |
| [67] | GaAs | Stacked | compound | 28 | 3 | 28.5 | 37 | 14.4 | mm-W |
| [73] | GaAs | Stacked | E-mode | 30 | 3 | 28.2 | 27 | 15 | mm-W |
| [74] | GaAs | Stacked | Stacked/N=3 | 3.6 | 0.5 | 42 | 41 | 20 | RF |
| [75] | GaAs | Stacked | integrated circuit | 1.95 | 0.4 | 28.5 | 41.2 | 30.6 | LTE |

application of the communication system. In this section, a set of these technologies and their objectives will be mentioned without delving into the intricate details, as that is beyond the scope of our research.

### *4.1. Power Combining*

In several areas of electronics and telecommunications, power combining is a method used to combine power from multiple sources to improve the overall output power. This method is very useful in situations when high power is needed for efficient signal transmission over long distances, such as in wireless transmission, satellite communications, and radar systems. These are a few research papers on various methods and applications for power combining techniques in electronics. A modified distributed power combining technique is used to create a millimetre-wave power amplifier. In order to improve power distribution and bandwidth without phase variation, the suggested architecture combines zero-phase shifting transmission lines (ZPS) with single-ended dual-fed distributed combining (SEDFDC). With an output power of 20.3 to 24.2 dBm and a power gain of 12.9 to 21.8 dB between 26 and 56 GHz, the amplifier is appropriate for 5G applications[77]. Another study presents a dual-mode power amplifier with a parallel power-combining transformer (PCT) designed to improve efficiency and linearity. The amplifier uses a low-loss transformer to enhance passive efficiency and an IMD3 cancellation method to reduce distortion. At frequency of 0.91 GHz, it delivers an output power of 33.8 dBm and a peak power added efficiency (PAE) of 54.5%, demonstrating its efficiency for high data rate wireless communications [78]. Another study examines a lossless multi-way outphasing and power combining system for microwave power amplification, aiming to attain nearly resistive load modulation across a 10:1 output power range with W-CDMA signals, the all microstrip implementation exhibited a peak drain efficiency of 70% and an average modulated efficiency of 55.6%, demonstrating its efficacy in microwave power amplification[79].

### *4.2. Linearization Technique*

To reduce nonlinear distortions in RF amplifiers and other RF components, linearization techniques are used in RF (Radio Frequency) communication. Numerous causes, including signal modulation, non-ideal operating circumstances, and device nonlinearities, can result in nonlinear distortions One common nonlinear distortion in RF amplifiers is called intermodulation distortion (IMD), where signals at different frequencies mix within the amplifier and produce unwanted signals at frequencies that are the sum or difference of the original frequencies. IMD can degrade the performance of RF communication systems by causing interference and reducing signal quality [80-85].

### *4.1. Efficiency Enhancement Technique*

To Improve the overall performance and energy efficiency of network, it is essential to enhance the efficiency of power amplifier. Numerous techniques are commonly used in 5G RF power amplifiers to improve efficiency include Envelope tracking (ET), Dynamic Biasing, Digital Pre Distortion (DPD), and Efficient Power Combining or Outphasing such as Doherty combining. The incorporation of efficiency enhancement methodologies in the design and implementation of 5G RF PA has the potential to elevate efficiency levels, hence facilitating the development of 5G networks that are more economical and energy efficient [86-90].

It is essential to note the future challenges in power amplifier design to determine the future direction of power amplifier design, according to the authors' knowledge.

Future power amplifier (PA) design for beyond-5G faces challenges from higher frequencies (FR3 and sub-THz), massive arrays, and stricter efficiency–linearity tradeoffs. Key trends include new device technologies, digitally enhanced architectures, and advanced linearization schemes. Co-design of PA, antenna, and tunable matching will be vital, alongside thermal management and sustainable operation in large arrays. AI-driven modeling and real-time adaptation are emerging as enablers for robust, efficient, and reconfigurable PAs in future communication systems.

## 5. CONCLUSION

This research aims to provide appropriate reference for students, designers, and professionals working in the field of power amplifier design,

offering a comprehensive summary of design technique for the most successful power amplifiers for advance communication system. This study reviews numerous research works that have examined the study and design of power amplifiers with in contemporary communication systems for the fifth generation and beyond. The topic was addressed on three levels. The first level focus on the transistor, highlighting the importance of transistor technology on amplifier performance in terms of output power, operating frequency, and even production cost. The circuit level is covered in the second level, which emphasizes the role that circuit configuration has in enhancing amplifier linearity and expands the bandwidth, reduce power losses, and enhance efficiency. To optimize the amplifier's operation and prepare the modulated and amplified signal for transmission through the channel according to communication system specifications, a third level of improvement is added. Enhancement techniques are discussed in the fourth section of this research, including power combining techniques, linearity improvement techniques, and efficiency enhancement techniques. The optimal design depends on balancing the amplifier's performance level with the complexity of the amplifier circuit.

## Nomenclature

| | |
|---|---|
| $fT$ | cutoff frequency |
| $gm$ | transconductance, |
| $Cgs,$ | Gate source parasitic capacitor |
| $Cgd$ | Gate drain parasitic capacitor |
| $Rg$ | gate resistance |
| $f_{MAX}$ | maximum frequency |
| $ro$ | output resistance |

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