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A Review for Faults Recognition in Analog Electronic Circuits Based on a Direct Tester Board

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ABSTRACT

The detection of faults in electronic circuits is crucial to ensure the proper performance and reliability of electronic applications that utilize these devices. This work discovers, for the first time, that a direct tester board for fault diagnosis can be used not only for the intended measurement of current and voltage but also for studying the potential development of these magnitudes in inaccessible locations, as it detects register transfer level signals through oscilloscopes with low acquisition speeds. The experimental analysis carried out combines the use of commercial software with spatial distribution tracking and the exploitation of the sizes of network links in their computer graphical representation. The proper detection of malfunctions in electronic systems is crucial for enhancing their performance and reliability. We intend to explore the troubleshooting of analog electronic systems, for which we use wide-band direct tester boards. To evaluate its performance in routine practice, we perform experimentation using two different analog circuits designed. They consist of conventional operational amplifiers and element modeling based on equivalent resistance-capacitance networks. Given the procedure followed, commercial programs were used. Special mention should be made of the conclusion matrix, which is interesting when selecting suitable diagnostic parameters. The effectiveness of direct measurement based on integrated probes in the two projects, which allowed for fault insertion, was also confirmed. The results and discussions were enriched by the summarized experimental test report. The work concludes with a reflection on the relationship between this work and the existing state of the art, as well as the new challenges posed by international researchers.

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1. Introduction

In general, fault diagnosis is an activity that utilizes expert systems, automation, and tests to identify the causes of failures differently from the failure warnings. As the test methods progress, particularly the DFT concept, which has two main objectives. The first objective aims to reduce to an acceptable level the task of checking the functioning of any circuit at any moment of its life in terms of external terminal truth tables, with a complete check suitable to detect the probability of malfunction also due to changes in threshold levels or changes in output impedances of generators or a dynamic increase in consumption [1][2][3]. The second objective is to check and control the correct implementation of a chip in terms of IC chip input or output logical level status; for implementation, IDDQ control must be added according to the common evaluation that the static component consumption of IC chips is about 10% of the dynamic consumption [4][5].

Automatic Test Equipment, such as digital pattern generators, digital logic analyzers, and oscilloscopes, are tools designed for fault simulation testing at the pin level of integrated circuits. However, to utilize such techniques in traditional testing, we need to connect external devices to the card on which the IC has been mounted, particularly for prototype and development analysis. The result is an increase in the cost, slowness, and loss of flexibility in circuit modifications. Some manufacturers frame this concept in terms of manufacturing costs, indicating that even 99% fault coverage can result in the testing cost exceeding the cost savings achieved through the use of advanced and high-integration techniques in manufacturing. The design, planning, realization, and implementation of an intermediate tester board is useful to check the functioning of a limited number of analog circuits directly on the printed circuit in real time, with very low hold-up times and with an investment of about 10% of the amount necessary to make a card instrumented with test pins set to be interfaced in a hypothetical Automatic Test Equipment [6][7]. This has the aim of acquiring information that guides us in the mounting of micro-card maturity tests, as classifications resonate in physical or functional sections, adjustments to be made in order to reduce as soon as possible the working percentage; it helps to open, following a temporal priority-driven rule, the watchdog before the moment in which the functionality decrease leads to missing classifications not foreseen by the model affecting the IC inputs as the correct inputs to be used [8].

1.1. Background and Significance

The lifetime of automated electronic systems can increase dramatically depending mainly on the efficiency of the test strategies. This fact is evident especially when the manufactured system fails, which may cause serious accidents or even death. For this purpose, within the qualification of an analog electronic system, testing is conducted by verifying the functionality of non-digital components, as well as the specific functions of digital circuits, such as digital-to-analog converters, analog data acquisition systems, power amplifiers, and others [9, 10, 11]. Thus, many techniques used in digital circuit testing can also be employed in the testing of other electronic equipment. In the development of this work, some methodologies were studied to test faults in analog electronic circuits, which may have been implemented in the digital form. These techniques, although well-established, still lack a testing methodology suitable for any technological degree at which they are implemented [12] [13] [14].

This work provides a contribution by using genetic algorithms with similar work in the testing of analog circuits. The present work aimed to propose a deterministic technique of automatic testing to be implemented in the electronic board to which the set of integrated circuits is attached, facilitating the tests, reducing the test time, the cost of maintenance, and minimizing the number of engineers and technicians needed to perform maintenance. These and other benefits are related to the various phases in the reliable operation of an electronic system [15]. By automatic and deterministic, it means that the tested system must not receive stimuli that may infer a semi-automatic or non-deterministic operation [16]-[19]. That is, a manually operable dedicated system that performs the tests in a totally isolated manner, without exposing the person responsible for the test to the possibility of a malfunction, such as a sequence that alters the expected behavior of the equipment.

1.2. Research Objectives

To achieve the aim earlier stated, the following more specific objectives are formulated:

Revision and remediation of computer algorithms for the analysis of analog signals based on the discretization of the transformation instead of just the transformation itself, as well as its presentation and decompression, reducing the loss of useful information closely merged to the errors we want to detect and measure.

Review and develop a better and more effective way of driving the AD converters than the zooming method commonly used, using for this purpose the

approximate band of the signals and the fast Fourier transform algorithm.
Study the potential and behaviour of analog signals under conditions of normal operation and a wide variety of possible fault types and causes that could occur in the analog devices based on the theory of complete models.

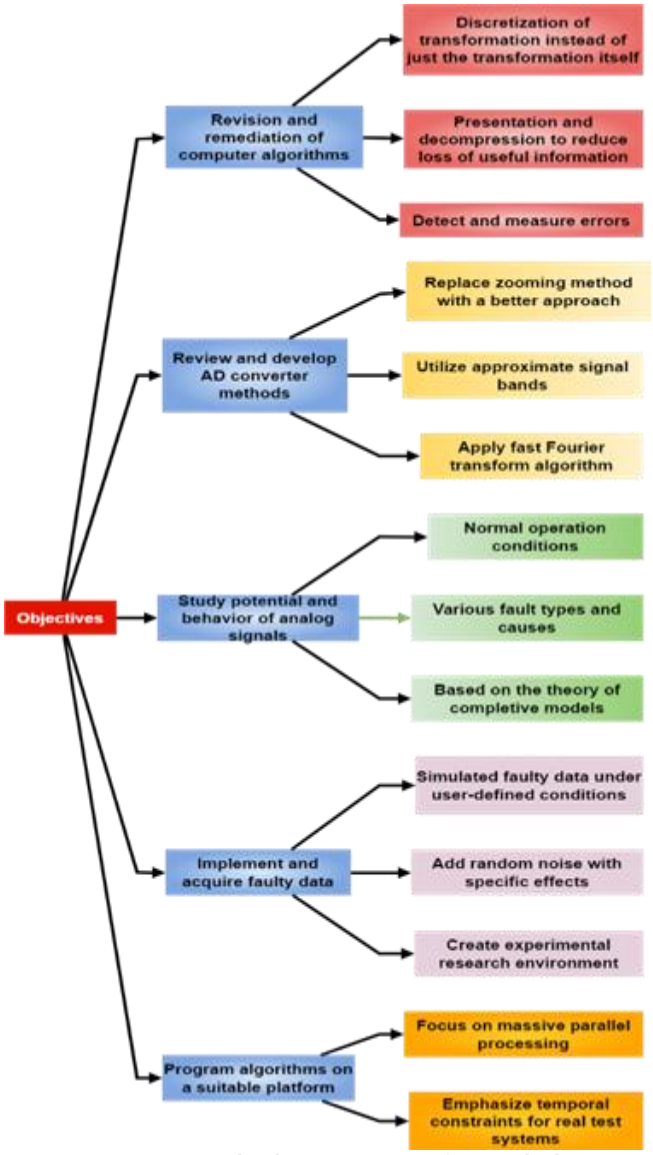

Figure 1. Hierarchical Representation of Research Objectives

Implement and/or acquire simulated and real faulty data under user-defined conditions to add random noise with specific effects and the experimental environment needed in the research tasks.
Program the algorithms on a suitable platform with special emphasis on massive parallel processing and the temporal constraints required by real test systems. Figure 1 illustrates the structured breakdown of the research objectives, detailing the key focus areas, including algorithm revision and remediation, enhancement of AD converter methods, analysis of analog signals, acquisition of simulated and faulty data, and programming on suitable platforms with a focus on parallel processing and real-time constraints.

1.3 Fault Detection in Analog Electronic Circuits

Current electronic system applications are extending their functionalities and requiring greater performance. These demands stimulate the development of high-performance integrated systems. These systems are constructed using digital electronic systems; however, in several applications, digital systems must interact with the analog domain. Examples of these interactions include power management, audio processing, interfacing with sensors or transducers, and interfacing with the real world. For many critical applications, the competence of electronic systems has a profound influence, in which performing analyses of a device's quality is vital [20] [21] [22]. In this context, these instruments can be used to evaluate system quality from the perspective of Analog Fault Definition, Verb Descriptions, and syndromes for the analog fault model and generic techniques and their properties [23] [24].
In this section, the fault detection problem is studied based on the original tester, named Direct Tester, which is functionally unconventional. Using the simulated test, the implementation gives 100% coverage and only one resistor per word of the test. This daily information is crucial because it directly impacts the test's efficiency and the system's cost [25] [26]. Many proposed circuits and methods are widely tested and have been used multiple times, with successful applications over a long period. This is the critical reason that the tester uses an economic analog card and regulates itself for switch times, whether intentionally long or not. Such doubts and misconceptions gave rise to a perhaps excessive overvaluation of the multiplexed analog tester or triggering circuit, which was manufactured in the digital domain and controlled by a numerical sequencer. These facts define the cutting edge between the context of 1973 and the present day [27], the second look, from the beginning of 1994 until the present time [28].

1.4 Delay Fault Testing and Diagnosis

Note that the delay fault is defined only for combinational circuits. Structural testing and detecting delay defects in the presence of any sequential element are complex. For sequential circuits, the built-in self-diagnosis is the main technique used for diagnosing delay faults. Sequential circuits have behavioral or functional

aspects that are the cause of interest, as well as temporal aspects, creating state diagrams or time descriptions, such as testing sequences and time-oriented performance [29]-[31]. The detection of delay defects in the functional behavior of sequential circuits is an increasing problem as the frequency of the architecture increases. If delay defects in the functional behavior of a sequential circuit are not detected, the structural technique cannot detect the transition fault in the circuit [32].

All sequential circuits have internal state elements that latch the inputs or the outputs for the delayed generation process. The detection of delay defects at the latched outputs leads to the testing of delay faults in combinational circuits. Sequential circuits can exhibit two different behaviors: combinational behavior or sequential operation. In tests designed for the detection of delay defects, the existing in the operation of a clock is associated with the state of each memory element, which prepares the initial conditions for the test sequence execution. Three additional subtests must be used to isolate the transition defects in the functional behavior of the circuit. [33][34][35]

1.5 A Review of the Direct Tester Board Analysis

This section reviews the major studies on the tester board development for analog circuit faults. Our review found that all these studies employed some form of a commercial PCB or vero board. Some knowledge is needed in the actual production of the tester board for its application. The method for adding the tester board to the system under test is required. All prior works have addressed the electronic analysis part of the tester board and have provided some form of fault diagnostic capability during their construction. The tester board provides only some form of analog fault awareness, e.g., openings, shorts, and shunts during construction.

The only fault identification provided is during the configuration of the tester board itself. The tester board derived from this project only provides a way of comparing the signals in the desired case with those for the actual. Additional results are needed to report the faulty state of the system under test. They are compared to the desired state; please clarify what these extra results are. With regard to the actual fault detection, analyzers, which are PC-based, high hardware cost, time-consuming, and complex, are employed. However, construction costs can be minimal with a low-cost, quick-to-build, easy-to-modify, and use tester board. With desirable properties, scalability can be addressed, e.g., the number of pins given in the address bus and ISA code defined by the architecture for an 8-bit structured target. A 4-channel version 1 board used for 4 address points is shown.

2. Fundamentals of analog electronic circuits

An analog electronic circuit is a device that is employed to produce electronic signals and operations in a continuous form. The consensus in the automotive, telecommunications, computers, scientific research, and important control processes for the industry is that the longer load depends on functions such as continuous, non-linear, complex use, and proximity to the use of electronic circuits. There are two emerging trends in electronics that are impacting this important method of prototyping and manufacturing.

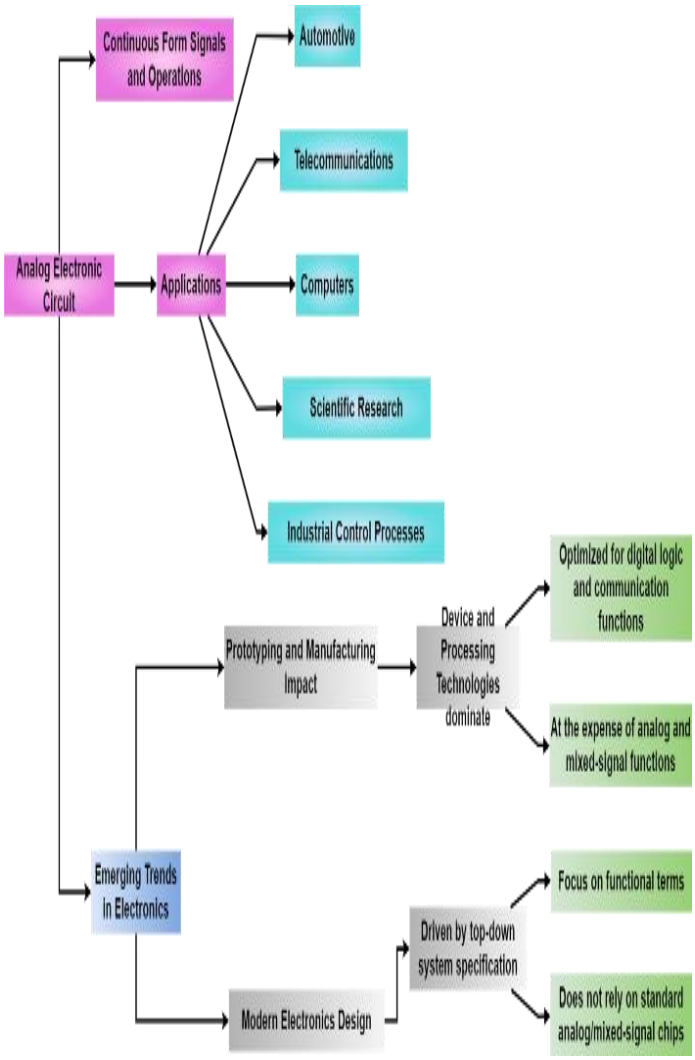

Figure 2 Overview of Analog Electronic Circuits and Emerging Trends

First, for prototyping purposes, at least, the device and processing technologies used are now

dominated by digital technologies, and these technologies are increasingly optimized for digital logic and communication functions at the expense of analog and mixed-signal functions [36] [37].
Second, in a trend that is increasingly becoming nearly universal for modern electronics products, the design of these products is driven by a top-down process that starts from a system specification written in terms of functions and does not express the solution in terms of already standard building blocks such as commercially available analog and mixed-signal chips [38].
In above figure 2 that illustrates the role of analog electronic circuits in generating continuous form signals and their applications across various fields, including automotive, telecommunications, computing, research, and industrial control processes. It also highlights two significant emerging trends: the dominance of digital logic and communication functions in prototyping technologies and the shift in modern electronics design toward a top-down approach based on system specifications rather than standard analog and mixed-signal building blocks.

2.1 Introduction to analog electronic circuits

The importance of analog electronics is primarily due to three fundamental facts. The first point is that the physical world is analogous, and therefore, all signals from the environment are analogous in nature [39]. The second one is that information processing within the nervous system has been accomplished using analog signals, and the third one lies in the mathematical properties of electric power functions, which are crucial for the efficiency of analog signal processing. The number of components currently sold in the market that work as embedded in electronic circuits of different types is very large, and most of these components work with electronic signals that are analog in nature, including microprocessors [40].
Although the present analog circuits have high integration levels, occupying only a small fraction of the silicon area, they still make use of a topology-type named operational amplifier for the execution of a vast range of typical or specific functions such as amplification or filtering. High-performance amplifiers can perform these functions in a much better manner, but at a higher cost, being no solution in those application cases for which it is possible to use operational amplifiers. It is important to observe that operational amplifiers are incorporated in the design of fundamental communication systems like telephony, and well-known physical effects existing in the circuit board, which supports these amplifiers, are responsible for the early noise among voices. [41][42][43][44]

2.2 Circuit Components

The fundamental components of analog circuits include resistors, capacitors, inductors, operational amplifiers, voltage and current sources. Generally, their relationship is represented by linear and non-linear differential and algebraic equations (Figure 3). The diode, bipolar junction transistor, and the metal-oxide semiconductor field-effect transistor are the most common and fundamental elements in semiconductor analog circuits. The connections between the terminals of these components were made based on the device physics and characterization. Depending on the connections, the terminal voltages and currents, as well as their mathematical relations, may vary. High-frequency and high-frequency equivalent circuit models for the active devices are essential in the investigation of the transistor for failures. In general, these models can be represented using equivalent circuits that mainly depend on the characteristics of the elements. The elements represented are capacitors, inductors, and resistors, and these depend on the connections between the transistor terminals. The adequate selection of the device and the equivalent circuit models to be used for fault detection requires the creation of a methodology based on fault simulation in bipolar transistor circuits. In numerous applications, depending on the terminal voltage, with credible reasons, it may be assumed that the transistor is an open circuit or a short circuit whose resistance depends on some design factor [45]- [47].

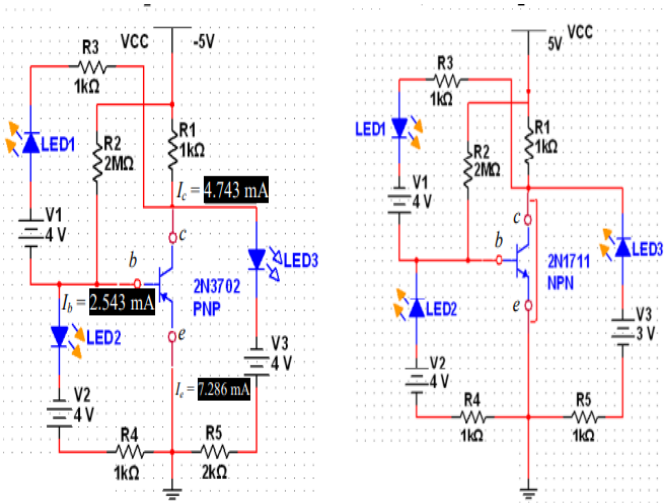

Figure 3. 1 The circuits' initial section for verifying each electronic component separately.

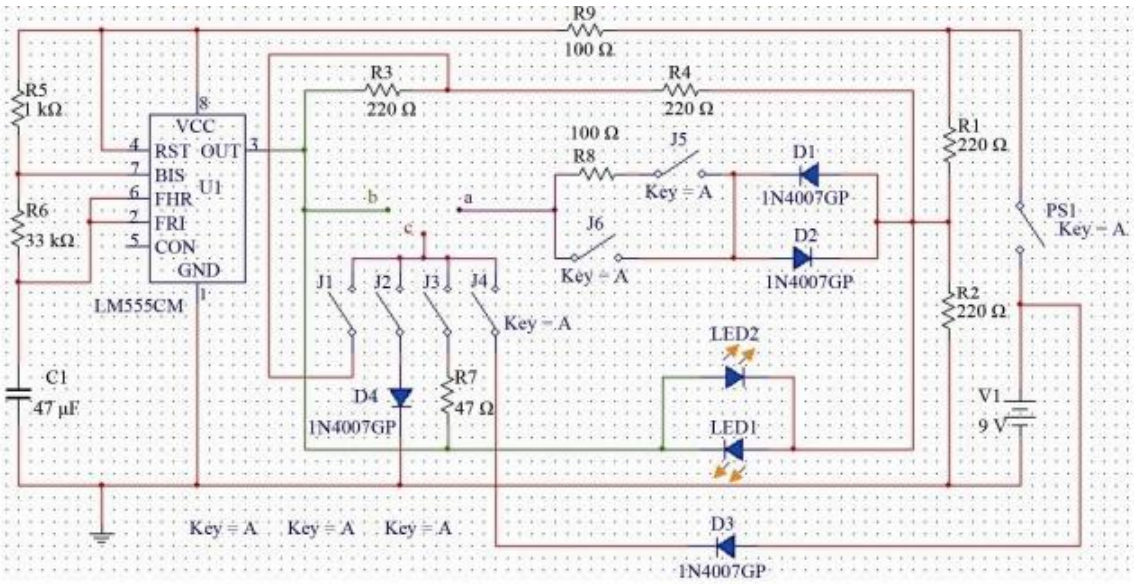

Figure 4. Simulation of model

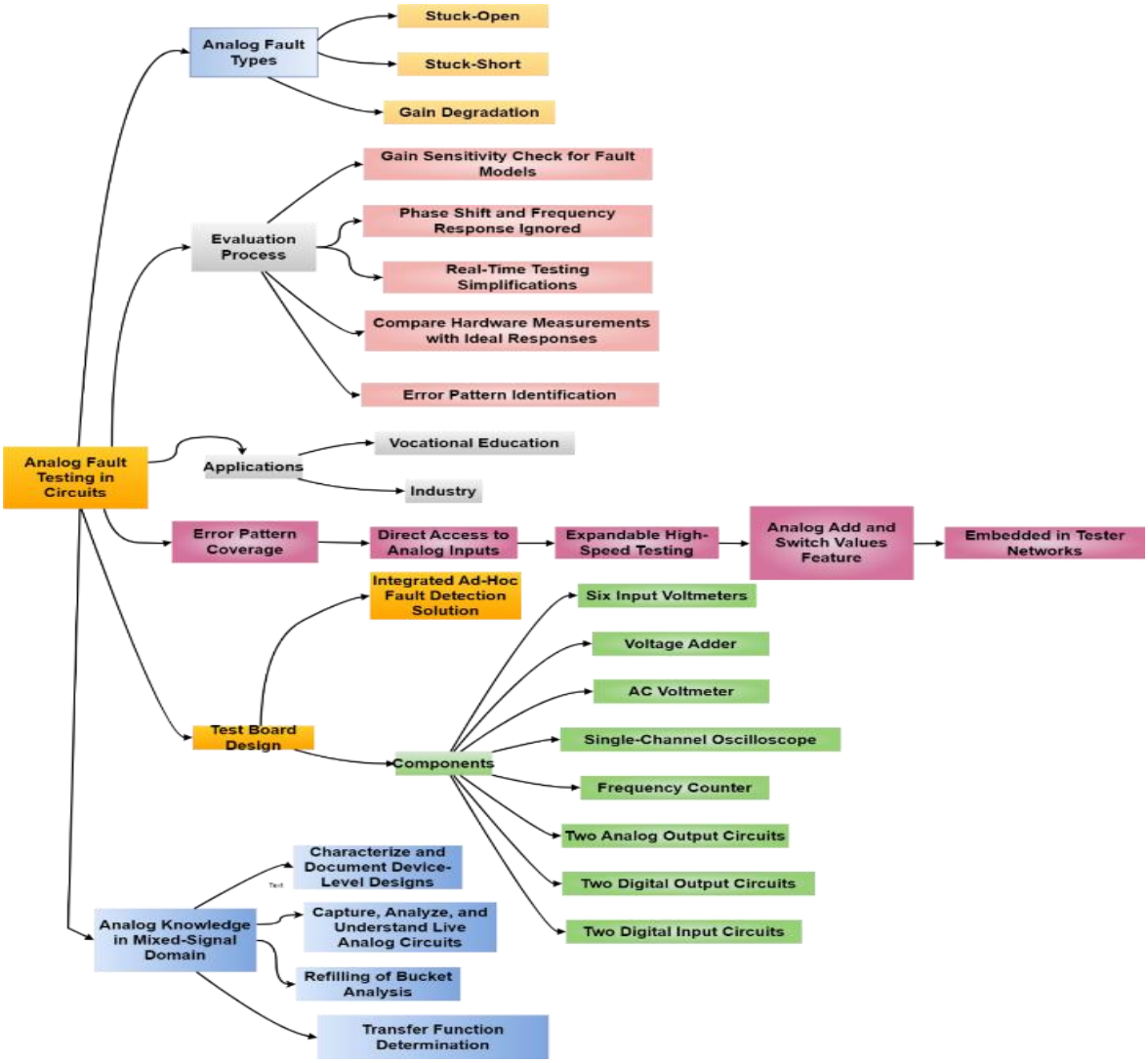

Figure 5. Comprehensive Framework for Analog Fault Testing and Test Board Design

3. Fault Detection Techniques

In circuit testing, analog faults, particularly stuck-open, stuck-short, and gain degradation faults, can be evaluated during the gain sensitivity check, which accounts for dominant fault models. However, phase shift and frequency response of the analog building blocks are completely ignored. The complicated high-level analog simulations are replaced with real-time testing simplifications. The hardware measurements are compared with ideal tester responses for error pattern identification from the ideal fault-free behavior. Vocational education and industry are the two areas in which analog fault identification technology is crucial for proper circuit operation.
Direct access to analog inputs in order to modify an expandable high-speed testing can then achieve error pattern coverage. This is achieved through using the analog add and switch values feature of analog multipliers, which are embedded in tester networks. The test board is designed by integrating the ad-hoc solution for fault detection of all kinds of challenges into the tester. The design plan highlights a direct board with six input voltmeters, a voltage adder, an AC voltmeter, a single-channel oscilloscope, a frequency counter, two analog output circuits, two digital output circuits, and two digital input circuits. Analog knowledge in the mixed-signal domain is fundamental while characterizing and documenting analog device-level designs. Capturing, analyzing, and understanding live analog circuits, and based on analog output, provide the design features. The refilling of the bucket analysis and transfer function determination of analog circuits is made viable with the direct tester board [48] [49].

3.1. Traditional Methods

As pointed out, the traditional methods for fault diagnosis in analog circuits can be divided into two categories: those that use the response to a range of input stimuli for each test of a circuit and those that only use the individual response of each output in response to a single test stimulus.
The first method belongs to the category of vector-based testing,
The second method is also called the watch-point technique.
In summary, vector-based testing strategies are broadly categorized as multi-domain testing, joint time and frequency domain testing, and multi-value testing [50]. The watch-point technique, which examines each output's unique response to a single test stimulus, and vector-based testing, which uses the response to a variety of input stimuli, are the two primary approaches into which this figure 6 divides conventional fault diagnosis techniques for analog circuits.
The vector-based analysis of analog circuits performs a vector of input and a vector of output responses for each configuration of the circuit. The proper circuit behavior is characterized by traditional measurements, such as the transfer function, impulse or step response, frequency or impulse sensitivity, and input and/or output frequency response [51] [52].

These techniques might assist a fault diagnostic algorithm. In fact, the most efficient tools for diagnosing a set of faults using signal features are change detection techniques and clustering techniques. These fault diagnosis techniques, applied to functional tests, are also known as residual techniques based on the analysis of the fixed part of a linear system differential equation model, which estimates the changes in the circuit parameters. The generation of the reference values is a fundamental issue and the main factor affecting these strategies. Therefore, these techniques may not be enough to help in the test response analysis of circuits, which naturally presents highly variable features due to the changes in the circuit transfer function [53] [54].

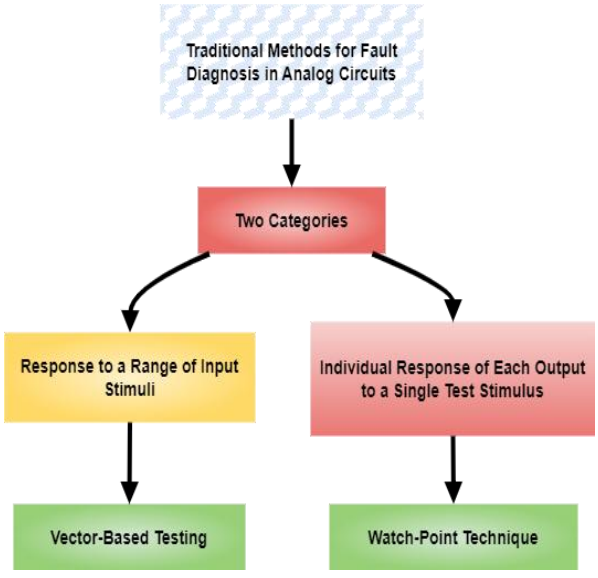

Figure 6. Traditional Methods for Analog Circuit Fault Diagnosis

3.2. *Advanced Methods*

In this section, advanced methods are briefly reviewed, as the details of some of these methods are presented in the introductions of the reviewed papers. This review only provides the context of the introduction, whereas the reader can find all required details about the studied work, including motivation and contributions. The necessity and state of the art of each proposed method are detailed and explained in the results and discussion sections.

According to the achieved review, the advanced methods proposed for fault detection in analog electronic circuits are as follows:

A universal fault detection method is dedicated to the employed board for the practical realization of the given approach and the advantages invoked by the proposed method; a custom method involves hands-on work based on the specifics and knowledge/experience about the circuit in use, as well as the significant creativity of the engineer involved; a brilliant method that is not a simple combination of the two previous approaches, but a part of an optimal and practical way of implementing any of these two methods. Moreover, a very recent fault detection approach designed a fault detection and isolation scheme based on machine learning as a decision-making tool in domains such as artificial intelligence. This approach focuses on formulating decision problems in terms of optimization problems and designing efficient procedures that provide nearly optimal solutions to these problems with relatively little computational effort. The associated properties of learning and how complex intractable problems can be analyzed by focusing attention on some carefully chosen sample problems and identified solution procedures are also addressed. [55] [56] [57].

An overview of different fault detection techniques in analog circuits is shown in above figure 7. These techniques include the dedicated method, which emphasizes board-specific benefits and practical implementation, the custom method, which depends on the engineer's creativity and hands-on work, and the smart method, which best combines the two earlier techniques. It also presents a contemporary method for fault identification and isolation that uses machine learning as a decision-making tool. It emphasizes the design of optimization problems, effective problem-solving techniques, and the use of properly selected sample problems to analyze complex difficulties.

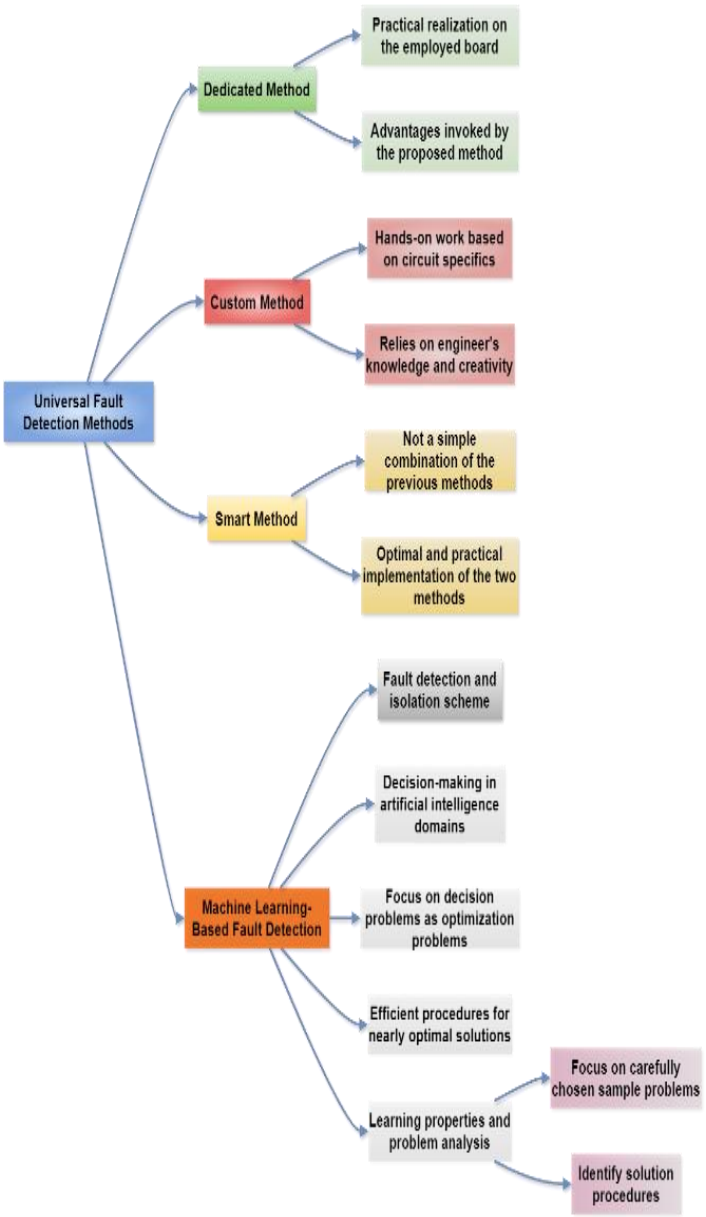

Figure 7. Modern techniques for analog circuit fault detection.

3.3. Delay Fault Testing and Diagnosis

For delay fault testing, as the proposed resistive fault model combines the parallel and series models, the RAPID rule is still retained for delay fault detection and analysis. The proposed detection method stands high as the defects to be detected may have a considerable effect. The only

thing is that the test vectors, whether they are ramp input vectors or not, may not ensure high transient voltage unless the delay fault is exactly located at the detection point because, due to the effect of low nearest resistors at high frequency, the ramp signal may not be strictly followed in a perfect form in the circuit output of the fault-free version of the circuit under test. The output patterns may still remain high, as the characteristic output patterns retain their nature, which varies with the delay fault [58] [59] [60]. 1) the ABSV measured at the fault increases or decreases. 2) the delay decreases. 3) the positive slack at the launching flip-flop decreases. 4) the positive slack at the capturing flip-flop remains the same. 5) the transition time decreases.

Additionally, the detection of delay faults and the extraction of information about the detected faults are made possible by relaying four pairs of outputs from the first derivatives to the test station. RCC is provided to become level 0, forcing its adjacent logical values in order to promote accurate testing. In diagnostic testing, FIFO is not used because if there exist any shorts, the AND gates constructed with data are useless. The structure was proposed directly throughout the diagnostic process to accelerate the diagnostic time.

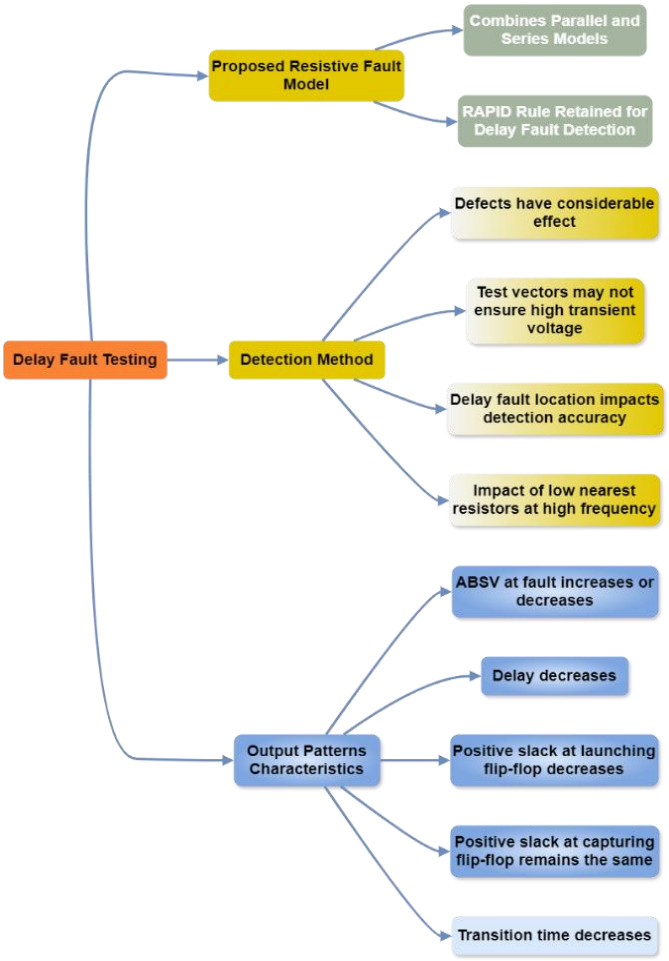

Figure 8. Delay Fault Testing and Detection Method

3.4. Path Selection for Delay Testing

Selecting paths for delay testing in digital circuits depends mainly on the heuristics implemented in the logical model of the circuits. However, ARC testing must apply knowledge about paths with electrical properties strongly connected to the technology in order to select the best procedures for applying stimulus and measuring observables. The sensitivity of the transition delay of the path to the variation of technological parameters is a criterion for ARC tests. Paths are selected in the order with the greatest sensitivity to delay variations. Transition delay testing selects paths by logically connecting sources with appropriate means to output enable signals in the output interface of multiple gate circuits. When a certain path, called a comparison path, becomes the longest path from the launch flops for up-switching all-fault detection, the inputs of the comparison path and the buffers of the comparison paths are connected to the non-faulty paths, and the longest path from the launch flops is assigned with a regular combination of comparators figure 9 [61] [62].

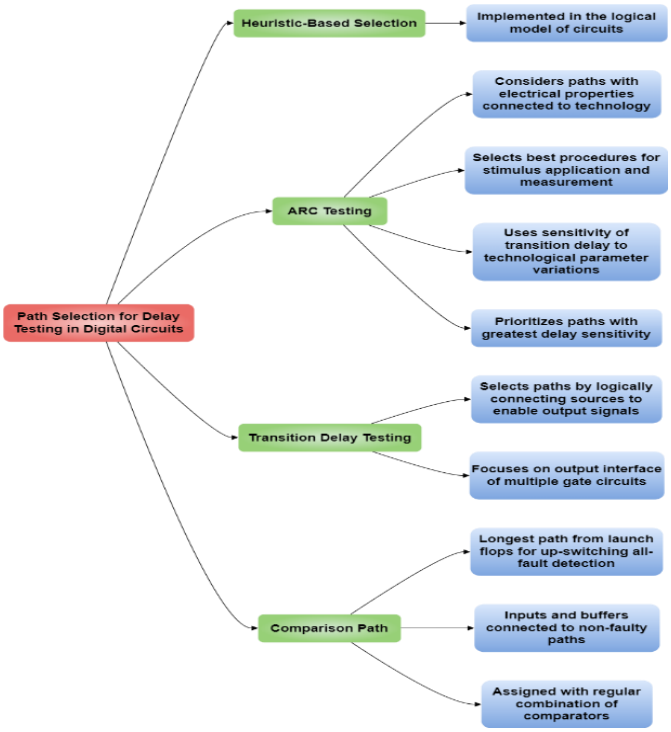

Figure 9. Path Selection for Delay Testing in Digital Circuits

A crucial problem in transition delay testing is the automatic determination of the comparison paths. Drawing all the comparison paths in line with the conventional design method is impossible because many internal nodes with redundant properties, such as stacked transistors for large output interfaces, will be required. When the comparison paths traverse the longest paths from the launch flops, the circuit test architecture can be implemented in a similar way with a test path of the slowest phase. However, we must consider the trade-off property that, while the comparison paths must be constructed using the regular structures as much as possible, they need the highest sensitivity compared to the other paths. The design tool we developed features an algorithm that takes into account the number of error signals appearing in the currently assumed comparison paths. We employ an algorithm that enables us to optimize the placement of the comparison paths without identifying the entire longest paths. Through the collaboration of these techniques, the reduction of the longest paths serves as a by-product, enabling all comparison paths to utilize the minimum average path length with regular structures [63].

4. Direct Tester Board Technology

This section presents the main features of the Direct Tester Board technology. The DTB is a reconfigurable device developed to support the implementation of the direct tester equipment. It allows the monitoring of any internal node and the application of test and diagnostic inputs in analog and mixed-signal integrated circuits. This system allows the direct interface with the contacts of a specific IC package before its use in the production of end-user electronic equipment. The DTT is based on a multimode, dynamically reconfigurable device composed of DC-gain amplifiers, sample-and-hold blocks, buffers, switches, and nodes for connecting other external high-level test and diagnostic systems or instruments. The DTT front-end architecture features a reduced number of dedicated nodes and a flexible access management mechanism, which saves space and prevents the limitations of independent direct connections with all the integrated circuit internal circuits under test. The DTT back-end was designed to redirect node signals, specific input patterns generated by an external system, and test and diagnostic clock modes to an input device terminal. This section provides a detailed description of the proposed system's architecture. The proposed Direct Tester technology is based on the development of a dynamically and adapted reconfigurable direct tester board. The design explores analog and digital adaptation techniques to reduce the number of circuit performance measurements required for some targeted electronic system specifications and to increase the number of implemented test challenges.

4.1. *Principles of Operation*

This section refers to the direct tester board of the review analysis procedure for classical fault detection in analog electronic circuits. The primary purpose of the procedure is clearly to support the educational activity. A typical application is the study or experimentation of the networking effect of components connected to the output of an operational amplifier. The testing procedure could include a suitable part of the teaching program for a basic analog electronic course. In particular, the procedure could be included after the conventional study of the topic and the experimental laboratory about that. Also considering the didactic purpose of the direct tester board, we must consider how the proposed application operates. The direct tester board is inserted in a simple testing bench with a regulated power supply always energized.

When the circuit switches, the operational amplifier energizes the turn-off pin and the real on/off pin, which allow the turn-off and the real inactivity state of the NMOS and NMOS, respectively. At the same time, the operational amplifier turns on the photo-coupler opto-receptor. The transmits light to the photo-resistor contained in another component. The photo-resistor energizes, with a power supply voltage of 5 V, the supply pins of the IC and IC, respectively, realizing the level conversion among 24 V, 12 V, and 5 V. The supply pins do not have the power required by the amplifiers, which are supplied by the input voltage divided by 2 via a voltage divider. realizes the voltage-controlled voltage source that feeds the thermostat. realizes the voltage-controlled current source that replaces the temperature sensor on the vocational training equipment. A buffer is used to verify the proper operation of the first component. The latter is used with the typical open-collector configuration and an NMOS is used as a current generator to feed a resistive inductive load according to the proposed topology, superimposed with the diode. When we want to simulate the occurrence of an electrical fault, we operate the switch lever.

4.2. Advantages and Limitations

Although direct tester development may yield useful tools for many applications, it cannot be applied to all types of systems. In many physical systems, the measurement activity itself perturbs the system, making such measurements intrinsically non-disruptive. Examples include faulty injector-based systems and hydraulic systems. Despite these limitations, the direct tester still offers several advantages over standard testing methodologies, instrumented test boards, and flexible external instrumentation. In particular, the embedded tester aims to address the needs of its primary user group, as

well as the versatile design and testing user groups. The key advantage of the direct tester is that it eliminates the need for expensive and disruptive test equipment, instead utilizing the requisite control and measurement capabilities found in many processors for normal operations. The direct tester, by creating elaborate configuration strings for individual components, can transiently fix states using the instrumentation circuit and confirm them by protecting sequences that were previously shown to have no harmful effects. The primary application of the direct tester, as its nominal user, is suitable for creating similar sequences without needing to visit the bench in advance. The direct tester also accommodates complex tests directly and flexibly, and can be performed at the same frequency as typical conflicting frequencies. Scanning tester increments are typically the longest points in a verification system because this processor does not have to dedicate processing resources to other user applications or to the test at the rated processor voltage.

4.3. Direct Tester Board Analysis

This section evaluates the direct tester board model-based fault detection method using two different AC tools. The detection capabilities, setter responses, time constant, leakage current, over-detection, and realistic testing conditions associated with the AC analysis are presented. For comparison purposes, the proposed test system is compared with the dynamic range and connectivity block analysis methods. A good detection is when the proposed method detects a fault that no other method can detect. The contrapositive test is also valid. Using a specific algorithm can help reach poorly grounded points, for which the practical tester bed cannot adequately measure the circuit, and thus obtain a poorly grounded measurement. This can be achieved by simply applying a relevant equation, which is already implemented in the tool. For both AC tools, the complete direct model is rich enough to produce the complex and often non-linear device behaviors, times, and currents necessary for the proposed fault detection application. Comparator output tests, for both the dynamic model and the collector current measurements, remain efficient and can be accurately determined to within a variable ground definition resolution of approximately 1000 points. These tests are fast, so that efficient outcome comparison and final test time requirements can be met, at the expense of high-speed communication and software and hardware systems that can be sufficiently incorporated to avoid incomplete or overlong test pattern scans. Rise times and fall times with orderly fast charging and discharging of the device collectors due to added biases can be inferred. The fine-tuning of the base currents and rise times to enforce the level-protected tests is fast enough to manage an otherwise predictable, unattenuated, and reversible global bi-stability. Fault responses to the tester.

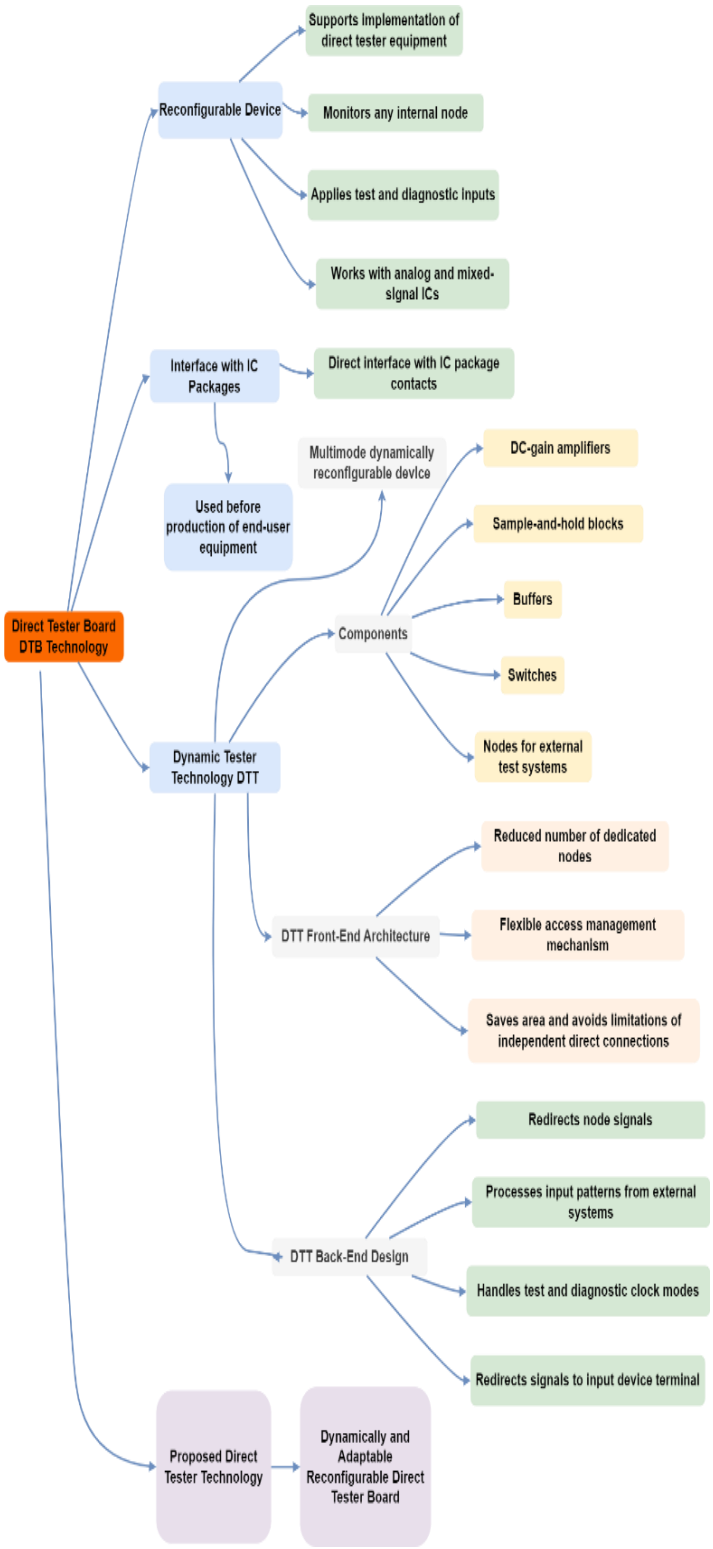

Figure 10. The diagram outlines the structure and functionality of the Direct Tester Board technology, detailing its components, architecture, and applications in analog and mixed-signal IC testing

5. Principles of Fault Detection in Analog Circuits

This section presents a detailed explanation of the principles, advantages, and drawbacks of the new method for fault detection in electronic circuits. Additionally, we demonstrate the operation of the proposed circuit. Finally, we outline the most critical limitations that will be considered for future research in the next section.

The principles of fault detection in analog electronic circuits are based on a new method. the analyzed circuit under test is directly connected with some commercial instrumentation to precisely control the voltage at the input of the circuit at discrete points during the designer-specified range. This battery of voltages is estimated using a system of memories, which is typically more costly than the wireless replacement technique mentioned for classroom or educational appliances. After possible amplification and filtering functions, the inputs of the tested circuit are driven by a multiplexer, which allows the selection of each memory block for the voltage control. With no interest in implementing more complex circuits, we assume the voltage is equal to zero whenever the equipment is not handling it. At the output of the circuit, the tester obtains the corresponding response and directs it to the corresponding facility, which is integrated with the test equipment used.

5.1. Role of Direct Tester Boards in Fault Detection

The role of Direct Tester (DT) boards in fault detection is to output test signals that allow the identification of potential faults in every part of the circuit under test. With typical DT boards, fault detection can be done by observing the variation of these test signals while the circuit is working correctly and by analyzing these signals afterwards. For instance, with the DT board for generating the reduced fault list, this task is achieved by an external system of neurons developed specifically for this purpose. This system, once trained, can detect the existence of a fault in the circuit under test by the observation of the respective digital outputs. Another approach, called the inverse look-up scan method, based on the well-known scan-path digital testing technique, seeks to identify where the analog fault is by means of the DT for fault detection.

Note that it is also possible to introduce a flow on the use of the information obtained from the digital outputs of the DT and/or neurons in further diagnostic reasoning over current and voltage oscilloscope traces to prioritize, in a more heuristic fashion, the remaining time-constrained testing steps.

The testing problem under study uses the same hardware necessary for fault detection when compared to previous direct tester designs, with the advantage that, because of the designer's need for the BD signal (already present in the test access mechanism), no extra effort is required during the implementation of digital testing to obtain a reduced fault list. In this way, the digital fault detection process used during the test phase, which precedes the fault simulation, is also accelerated. It is common to incorporate nonlinear digital testing with specific devices, chips—or, effectively, modules—when it is known that individuals working specifically with those devices can benefit from additional information about the responses. This concept can be extended to specific case modules focused on tests for dynamic fault detection in all these different types of circuits. In particular, when complex circuits have to be tested, a new test module should allow people to use the test information that is not actually exposed to test the circuits on the device itself.

5.2. Advantages of the Direct Tester Board Analysis

The current analog circuit's reliability verification occurs over exhaustive testing of devices equipped with a parametric tester and a direct current board, examining just a limited set of input voltage conditions. The proposed tester board is a better alternative to execute exhaustive tests specifically in the analog fault detection process. The features of the tester board are analyzed from the detected fault coverage values obtained from three different analysis approaches. The physical manifestation of the signal path isolation this proposed tester board performs and solves the modeling related problem. The loss scenarios as a function of the isolation path-independent path combinations are presented, and the lower power consumption will make the circuit work in high meantime between failures.

However, the cost of both development and service is expected to increase substantially because of the difficulty associated with using their embedded test after the fabrication response and the high cost of capturing and analyzing a huge amount of test data. Self-test methods are used to test semiconductor testing for the manufacturing environment in a cost-effective manner. This additional circuitry presents two issues: how to model the diagnosable circuit and how to develop diagnostic data that unfold the fault during self-testing.

5.3. Limitations of the Direct Tester Board Approach

Limitations of the Direct Tester Board Approach. There are several limitations to the direct tester board approach to fault detection. First, the nature of potential software or microprocessor fault capabilities themselves is such that they can prevent characterized faults from executing. This ultimately is not a limitation to the software so much as the method chosen to communicate the external electronic support to the subject circuit. The potential number of components is very high, and it is not feasible to cater for all possible types. In terms of component coverage, the type of circuit under test and any irregularities in the component packages may entirely limit the suitability of the approach. In addition to component coverage, there must be stylistic rules or constraints for the design of the circuitry under test. These rules prevent, or at least prevent, issues such as components being too tightly abutted.

As the system is powered up, the electronic system voltages will increase from 0 V full scale, i.e., the power supply turn-on voltage, and then undergo a transition period before remaining stable at a predetermined value. In most mixed-signal boards, the form of the test stimulus may need to be modified to enable the correct testing of power-up and power-down operations. For example, the majority of tests require interface protocols to be in place, such as reading and writing to certain test latches. This read and write and potential lack of precision on the stimulus is potentially an issue as the power lines increase from 0 V to their nominal operating value. In the deterministic switching pattern phase, a failure junction occurs when the current flowing due to a fault exceeds the quiescent current of a normal junction, resulting in an open circuit. As the system is powered up, the electronic voltages will gradually increase from 0 V to their nominal operational value. As the voltage is being driven to a constant value, digital systems may be at any number of states, voltage levels, at unknown logic levels. In the worst-case scenario, all the digital circuits are at mid-rail levels. The direct tester would not be able to apply a stimulus to force the transition from one state to another.

5.4 Comparison to Other Fault Detection Techniques

We present the results to compare the performance of the tester designed using the non-invasive technique with that of other fault detection techniques. First, the results indicate that this tester discriminates between SNR faults and other types of faults. Second, the percentage yield achieved by the tester is higher than that of the complete fault detection approach. However, the tester classified every BAR481 as faulty, including all the original components without any defects. Analyzing these components, we concluded that insufficient S/R was the reason for the classification fault. This disadvantage can be compensated quickly by using and modifying the approach with the non-invasive technique to produce a better calculation of the p.d.f. SNR models for the whole set of components. In conclusion, by using, modifying, or implementing new approaches to compute the various models of components, the technique can quickly produce a high-performance tester by achieving a combined high-test yield with a high-value classification fault.

Figure 11. Visualization of the tester's performance analysis, the identified issues, proposed modifications, and the conclusion emphasizing improvements for a high-performance

5.5 Trends in Analog Circuit Fault Detection

The applications of analog and mixed-signal electronic circuits in a broad range of devices and systems used in areas such as telecommunications, medicine, defense, and consumer electronics require

special attention in their verification, testing, and fault diagnosis procedures. The reduced number of controlled tests by equipment involved in the analysis and diagnosis of these circuits has necessitated the development of techniques that enable the detection of failures that are typically difficult to identify or that cause the circuit to exhibit incorrect behavior. Functional defects in analog and mixed-signal electronic circuits can result in low quality in several areas of application, compromising these systems and their applications. The development of innovative diagnostic technologies that operate within this range of circuits enhances the design, testing, and production processes of electronic devices and systems. fault detection is used to determine which component has failed. In analog circuits, it is necessary to produce as many signals as faults involved in the diagnosis. The main problem is acquiring the signals that can reveal a fault. This is a consistent problem, mainly for analog and mixed-circuit designs. This work presents the development of a technique to detect faults on actively loaded differential pairs with grounded loads and to identify the faulty component using the Direct Tester Board tool. The difference from the existing works is the unique solution presented to detect and identify circuit faults. The paper is organized as follows: the planned solution is presented, followed by some basic information, and then the procedures for detecting and identifying faults are outlined.

6. Applications of the Direct Tester Board Analysis

This paper aims to demonstrate the practical application of the Direct Tester Board (DTB) approach for fault detection in analog electronic circuits. A basic standard operational amplifier, in its differential, inverting, and non-inverting configurations, was targeted for analysis. A constant gain is set in each configuration. The tolerance of the resistors to deviations can be thoroughly investigated. Two restricted experimental ranges were used for component compensation and DTB testing. Both ideal and realistic prototypes can be parameterized. The mathematical calculations are always compared with a digital simulator for DTB production. The basic idea is to demonstrate how to apply the DTB for fault detection based on experimentally observed results, with a didactic objective for the R and A levels. The potential benefits that the direct scheme implementation can bring are also being observed.

The enhancement of the DTB approach for fault detection, based on thresholds and judged results per operation, can be configured under parameterized patterns. Such quantitative thresholds followed by qualitative maximum tolerances per passive component in a whole power amplifier are demonstrated as a considerable advantage for mass testing, where a green light can indicate a pass/fail test. The digital board tester protected non-soldering direct scheme approach has the true potential to disclose component deviations in crucial conditions. The several applications of the device under test for three simulations of bridge and differential measurement models and some case studies can essentially evaluate the experimental correction of a passive component to compensation schemes, basic instantaneous, and standard linear fault detection. Some indicative practical thresholds validation operational amplifier tests are further observed.

6.1. Theoretical Foundations of Fault Detection

When an analog electronic circuit is working, the output is dependent exclusively upon the parameters required by the analog circuit's theory. If these parameters are intermittently changed, this situation can be discovered from the results produced by a circuit because its behavior can be different from the expected patterns. Both the performance of an analog circuit and its behavior are closely related. To diagnose a faulty circuit, it is sufficient to compare the circuit's behavior with the expected behavior. In this study, the expected behavior was considered to be based on the parameters of the transfer function, which is an important type of characterization of an analog circuit, and also the tests applied to a certain implemented solution.

The possibility of detecting a failure in a symbolized and disassociated manner through the analysis of the transfer function or the analysis of test behavior is interesting to register before anything else. Faults can occur by different mechanisms, and the most favorable situation would be to exploit this knowledge to choose a single method that is able to verify all the possible lingering causes of repair. However, the number of combinations of the mechanics through which a component may fail is very high. Consequently, a method that can respond effectively to the detection of any type of failure looks increasingly far-fetched.

6.2. Experimental Methodologies for the Tester Board Analysis

During the development of the proposed method based on the DTB, some experiments were conducted to observe the feasibility and tune the variable values into the method. Initially, a set of 11 analog electronic circuits with single or multiple faults was gathered. The faulty semiconductors are associated with failures that can be developed with a hot source. In this way, laboratory experiments have replicated the damage. The hot source technique was used with a planar source based on an energy dissipator. The fault insertion procedures were carried out in 42

semiconductor devices, and the selection of faults was based on previous tests to determine the highest levels of entropy. Subsequently, a set of diagnostic rules divided into emphases in junction and dynamic resistance were established and classified into three levels of priority. Additionally, there was already emphasis on these diagnostic rules. The diagnostic rules classify different group types, including diodes, BJT, FET, and BFR. Then, based on the connections of each group, adapters were designed on a digital protozoa. In addition, purposeful measurements were taken for voltage, intensity, and the subsequent calculation of association resistance and time constants. Additionally, the professional multimeter connections for each set of measures relevant to the diagnosis were illustrated.

7. Data Processing and Interpretation Techniques

In the Gallery program, digital images of the printed circuit boards are obtained. The shape of the resistors on the tested board is rectangular or square, which can be easily identified with proper knowledge of their values. The Hough Transform converts the rectangular shapes of the resistors into their equivalent resistive values. One of the important parameters is the threshold value. This corresponds to the minimum number of points that should be found to correspond to the noisy pixels in the resistor segments to be able to recognize them. The resistor detection is robust to the presence of false edge points by a selection process incorporated into the Resistor class definition. All the errors arise due to detection problems caused by two clusters of line segments and short-circuited resistors.

Our general scheme for automatic fault detection and diagnosis of the analog filter's PCBs is to examine the relevant analog component performance for each module, periodically searching for any behavior that differs from that of the tested board. An inaccurate parameter threshold or suspicious parameter range is determined between two different available printed circuit boards on the same nominal values and the present on the board. Upon the detection of a circuit or a specific component fault, the identifier and location of any possible cause of failure are displayed using the principal component's value. These capacities can be accelerated by modifying the rules that define validity checks or parameter thresholds for specific combinations of component values.

7.1 . Challenges in Implementing Tester Board Systems

Considering that the test system is to be part of a manufacturing environment of electronic circuits and modules, which typically operates continuously throughout working hours, it takes into account the fact that this system becomes a computational and electronic processing system with low response times when stimulating circuits. The promptness of responses to disable any incorrect behaviors of test signals on the outputs of the circuits is important to avoid possible damage to the circuits themselves when driven in abnormal operating regions. The direct board tester system should have a sophisticated application for processing the board/counter-pin output signals. This application should be able to locate the instant of each known sequence of signal types when interested. In particular, it should have specific procedures that consider the context of each event identified in the sequences of signals. These procedures evaluate and store response values to excitation signals and make decisions about the circuit replies in the context of plain interaction in the circuit.

Because the application has to respond to each of the identified events in the sequences obtained by stimulating the circuits, rule expressions that monitor these events are described, as well as the register windows and interfaces used by these expressions. Due to the characteristics of these systems and each of their operations, it involves the utilization of a number of specialized resources, including data acquisition circuits with programable source signal directions, to test the physical model, memory management, as well as computational resources with an economically automatic attitude from the user's point of view. The design deals with fast activities mainly in real time. This design process could be guided by high-level specifications and synthesized to descriptions. The software components could be used to ease the technical development of the board, mainly for the specialized resources identified. Signal processing tools could allow porting the system for specific applications, as well as processes that combine the estimated robustness and scaling levels of the system.

7.2. Integrating Tester Boards with the Circuit Design

The aim of a tester board is to bring input signal sources and monitor the response to the circuit under test, as well as the digital fault detector algorithm in order to determine if there is a circuit fault available to a user. Thus, the main effort is integrating the tester board as well as its components into the existing circuit design and interacting with the user's design tools. The time taken to create a fault detection system determines the usefulness of such a prototype; therefore, decreasing it is of great importance. This can be achieved by integrating the fault detection functionality right from the circuit design stage. Resistive bridges are a common block found in many designs. Fault detection for these blocks translates to the same typical approach.

The digital CMOS resistive bridge implementation is compatible with typical tester board components. Existing design tools take advantage of typical foundry components such as inverters and buffers. A fault in a bridge occurs when a resistor node is disconnected from its corresponding bus and has no functionality. R3, R4, and the output node can be shorted to simulate this error. These cases can be tested during the functional circuit validation along with the resistive bridge verification. It is useful and can be performed exclusively for test. The results from the early stages of the design ensure that the end design of a fault detection system is a good engineering solution. Integrated fault detection components are the preparatory steps in creating a market for circuit designers.

7.3. Reliability and Robustness of the Tester Board Solutions

The combination of a pattern generator, a voltage buffer, a fault detection system, and a sensing buffer provided a functional prototype. Still, none of the presented universal board tester solutions were fully designed to be versatile enough to allow their use without the need for external equipment. Moreover, previously developed direct tester board equipment for particular fault detection, as subsets of the described equipment, are used for pre-processing and initial validation assessment. In this work, the ultimate objective was to assess its capabilities as a realistic, stand-alone fault detection solution. With the increasing difficulty of validation in testers designed for modern electronic boards, immediate automatic self-test capabilities are helpful.

Minimizing the external requirements and increasing the robustness and reliability of the solution are typical features in an authentic design for a test problem. With the increased fault detection load, it is expected that the user will utilize this solution for both stand-alone electronic equipment and cell phone-sized electronic components, as well as the respective development kit motherboard interfacing circuit starter kit devices. At the same time, the added development time, the increasing price of the units with the more complex circumventing equipment, and the requirement of a more extensive communication and interface resource library to deal with the larger quantity of offline connection equipment promote the user acceptance problem. The previously described hardware fault detection optimizations balance the above problem so that a lower total order quantity of different target application fault detection board solutions is designed to allow easy interfacing to the same, already existing, cooperation microcontroller board template.

8. Case Studies of Successful Tester Board Applications

This chapter presents four case studies of successful applications of the proposed analog fault detection platform. These case studies represent different types of hardware and software test systems developed, the possible in-circuit operation conditions, and real application scenarios of these test systems in different analog products. The case studies demonstrate the practicality of the analogue fault detection platform and facilitate the usage and understanding of the proposed platform.

The first case involves a machine vision-based calibration and testing system. Based on a digital camera and a standard signal processing board, this hardware test system can detect particular defects in the tested analog video cars. The second case study concentrates on an infotainment system. The design and development of an infotainment system suitable for the environment, testing the sound/audio section of the infotainment system with the provided tuner hardware test systems. The third case presents a mobile phone radio section test system hardware. The last case shows how to apply the tuner hardware tests with the software test systems. In this case study, a video capture card can be used to realize real-time testing. By capturing composite video outputs, the image of the analog video on the DUT can be treated as an observation signal, and relevant test algorithms can be applied to test the system health and identify malfunctioning circuits.

9. Future Directions for Direct Tester Board Research

In the past, some studies have presented studies related to the Direct Tester Board, using it to test digital electronic systems, introducing specifics about the boards used in experiments, and presenting an analysis based on Karnaugh mapping. Then, with the development of the boards available here, experimental studies were also performed, testing analog electronic systems for the first time, verifying the feasibility of the technique. This study investigated the results obtained for the various electronic configurations tested during the experiments carried out to offer suggestions when the Direct Tester Board is being used for this application. We also believe that there is potential in testing analog electronic circuits with more complex behaviors. Other possibilities may involve various other interface types, such as a board that selects the values of a transmission circuit and/or power supply to test all or part of a UUT powered by a battery. Although the designs can be easily adapted, converted, and might even be combined to form the so-called “Direct Tester Multifunctional Board,” all theoretical developments are as mature and proven as those already achieved in practical experiments. In

particular, maintaining them in an agreement process with scientific inquiry and the teaching-application process is essential. In this respect, many works in the form of documents, software, and summaries will be of interest. Only scientific and applied experiments will be able to enrich this cycle of new developments from the designs. Finally, we stress the importance of sharing, promoting, and inviting all those interested in collaborating with the developed designs and the data obtained in this research.

9.1. Practical Considerations for Tester Board Deployment

Depends on the height of the real circuit and tester board; it may induce bridging caused by the mechanical toughness. Hence, normally, robust mechanical test pins should be used, and long rigid bare wire links should be avoided. With robust mechanical test pins, consider the height difference visually and correct the position of the tester board and circuit for each test. Problems at this stage of the project will be significantly lower. For experiments, a laboratory notebook or a PC mounted on the tester board was used to log the readings and debug the implications of the results. The GUI should be used for the measurements.

The typical 0-5 V input from the signal generator or DAC will be connected to the character card through the test pins, as specified in the standard analog input section of the tester board user guide. The analog pins will be selected by programming the character card and using a SET command from an easy framework program interface on the PC, which serially interfaces with the board. After the test points are connected using the correct test fixtures, a controlled tester board manual measurement will be made using the multimeter, with the result being analogically interfaced with the character card and also digitally interfaced in the schematic on the card to detect the actual fault in the analog circuits. Depending on the schematics of the complex coupled analog circuits, the first tester board analog tester unit will be switched on, manual measurements will be taken, and recorded. Then, the analog tester 1 will be switched off, and vice versa. Through the observed measurements given repetitively with a normal determination-based t-test model, the test units will comment on which exact part of the analog circuits the fault exists.

9.2. Standardization and Regulations for Tester Board Use

Currently, there are no specifications to establish a common standard for the use of tester boards for analog circuits. This lack of standardization leads to different approaches for the design of the tester boards, resulting in products with different characteristics. The developed tester board is intended to be used in electronics analog education and fill this present absence. Moreover, the development of exercises and practical sessions in the electronics area for testing analog electronic circuits through the use of the developed test board helps students experience the operation of automatic test equipment during their early training, thereby familiarizing them with ATEs.

Regarding the use of tester boards for electronic analog circuits, there are currently no standards governing this area. The development of a standard is essential because ATEs are increasingly in demand in industrial processes. There is also a lack of tester boards that focus on educational purposes. In this work, attention is given not only to the cost aspect but also to the ease of development, construction, and repair. It is of paramount importance in the educational context to have documents such as diagrams, construction habits, test documentation for finished assemblies, and a code to obtain and modify the same. However, the usual tester boards do not contain such information. In addition, tester boards do not use virtual instruments, which today help make ATEs economical, which involve a curve tracer under its full load.

9.3. Emerging Technologies Impacting the Tester Board Analysis

Tester boards for fault detection in analog electronic circuits have been used consistently since 1940, verifying accuracy and resilience in many applications. However, some characteristics inherent to analog techniques, particularly the superposition of signals and design tolerances, may shift, altering deterministically expected measurements, which will impact the fault detection table of the board and may even generate false errors. This process can be accelerated by three groups of emerging technologies: technologies related to analog components, such as track and hold or bucket brigade devices; emerging technologies impacting analog techniques, such as fuzzy logic, which modifies the measured characteristics of time and frequency; and technologies related to measuring instruments, which can perform automatic functions to compensate for measurement distortion. Once the origin of the fault that generates the new measurement approach is identified, a significant part of the fault detection table can be recreated, and a new approach is established for analog techniques. The remaining parts of the fault detection table can only be modified manually. Assemble technological components to implement segmented or multi-resolution converters providing the ability to integrate a diagnostic test and improve performance, among them: types of classifiers based on analog techniques, evidence recognition mechanisms, isolated vertical thresholds with

integrated memory in ideal amplifiers, and identify and establish ideal manufacturing tolerance conditions. Create parametric models to predict the error of specific analog circuits caused by design tolerances, eliminating the need to fabricate integrated circuits for experimental verification. Mitigate the impact of analog design tolerances by intelligently choosing from one of three approaches: shifting the fault detection table, recalculating constants or test functions in use, or minimizing the usage of certain components in the diagnostic test.

10. Cost–benefit analysis of Direct Tester Board Adoption

Nowadays, early fault detection in production lines is essential to the success of any industry. There is a growing interest worldwide in increasing the reliability and reducing the maintenance costs of analog circuits, along with the increasing demand for electronic systems with a high density of interconnects. The electronics industry can utilize various techniques to directly detect faults in analog circuits. However, most techniques are based on the application of standardized tests, which involve high costs when the analog circuit is still in its prototype stage, especially in large-scale production. A cost-effective solution is the direct tester board.

The direct tester board allows for immediate fault detection, thereby increasing the productivity of the prototype production line in the industrial process. The components are tested according to the IC functional signal or pins. It involves low experimental costs, low implementation costs, and low complexity. It is independent of the power supply, clock, or any complex synchronization, and is portable and reusable. It does not require any active components beyond those dictated by the standard tests. It is also capable of performing universal ATE measurements, including functional and parametric measurements. Additionally, the signal acquisition is compliant with the tester requirements when the automatic test equipment becomes available later in the production assembly. This proposal presents a detailed proposal for a direct tester board. Its generality and potential application for testing complex analog and mixed-signal systems are illustrated. The results of the Universal Direct Tester Board are presented and discussed for an experimental application, including the test of an H-bridge.

11. Conclusion

The technique we have presented successfully integrates several essential features for fault modeling; specifically for the SD Method, it uniquely fulfills the three critical conditions necessary for effective operation: it defines well-established and clear operation regions of the circuit component under consideration, allows for a measurable time constant that is directly proportional to the specific component value, and provides an unambiguous and consistent input excitation. To effectively detect faults in straightforward electronic circuits at a designated test point, the designed tester circuit is exceptionally simple, and the programming of the tester board is designed to be straightforward as well. By employing the fault detection technique devised specifically for the tester board, numerous significant advantages are attained, including remarkable simplicity in both the construction and the programming processes involved. Furthermore, owing to the presence of just one time-constant measurement, this fault detection technique can effectively be made almost entirely independent of the propagation delay that may affect the circuit under test, thus increasing the reliability and efficiency of the measurements. By implementing the Direct Tester Board, it becomes possible to realize non-ideal element testers, which allows for considerations of real-world deviations from the ideal behavior in electronic components. As a result, the number of ports used in a mixed implemented environment for the systematic testing of a complex electronic system is notably reduced, significantly enhancing the overall efficiency and effectiveness of the testing process. This reduction in complexity is particularly beneficial for maintaining streamlined operations in both laboratory settings and practical applications, where time and resource management are crucial. Ultimately, the integration of these features leads to a more adaptable and reliable framework for electronic circuit testing, ensuring that accurate assessments and diagnostic capabilities are maintained throughout various operational environments.

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Conflicts of Interest

The authors declare no conflict of interest.

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